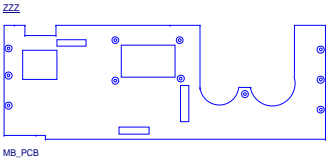


MODEL NAME : CAZ60
PCB NO : LA-E671P
BOM P/N : 43xxxxx



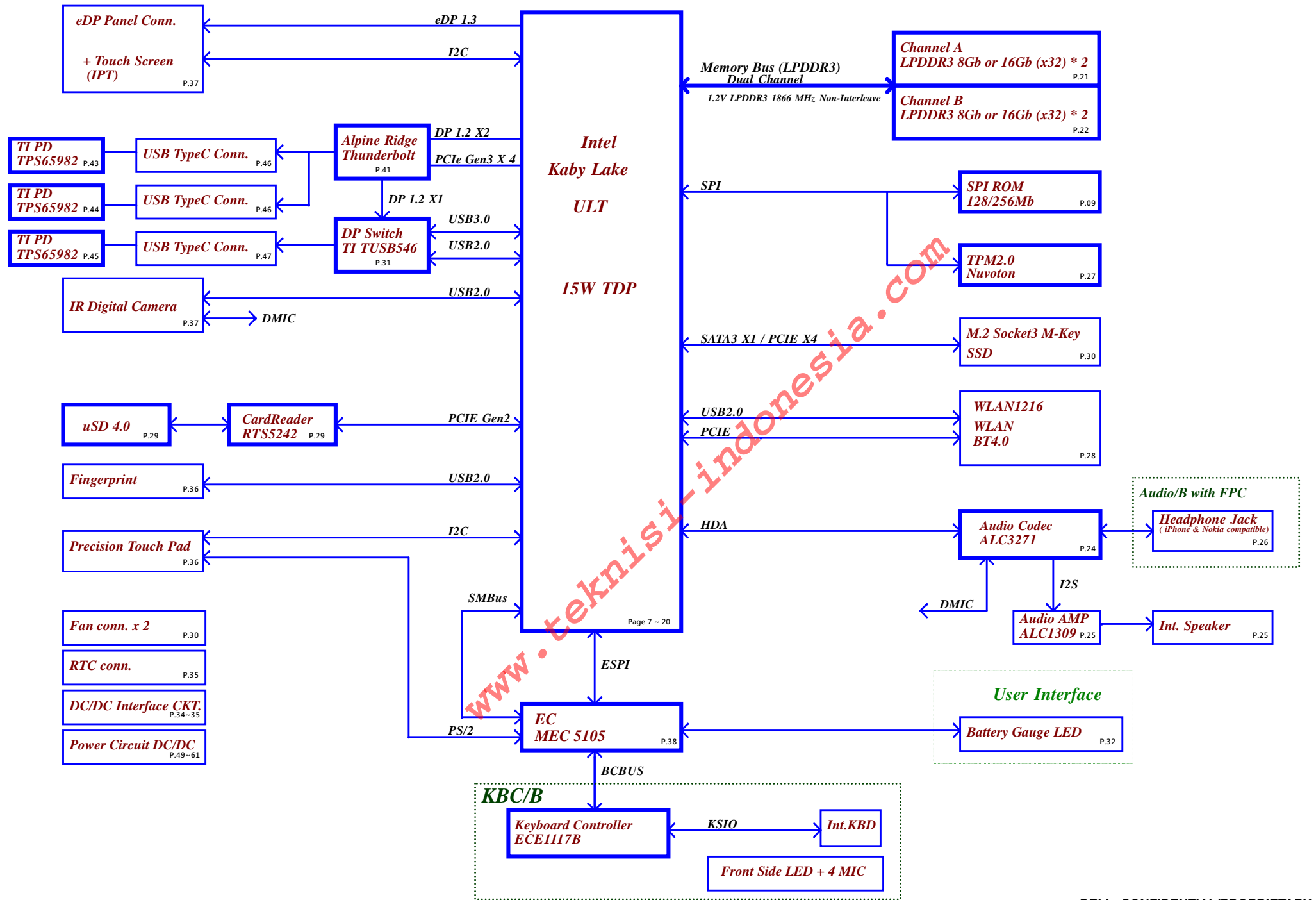
Dell/Compal Confidential

Schematic Document

Italia

2017-09-15
Rev: 1.0 (A00)

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Date:				Tuesday, October 17, 2017		Rev	
Sheet				1		1.0	
of				61			



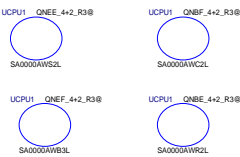
2+2 CPU Option



2+3 CPU Option



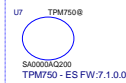
4+2 CPU Option



AR Option



TPM Option



DRAM Option

	UD41 M4G_1866@	UD42 M4G_1866@	UD43 M4G_1866@	UD44 M4G_1866@		MEM_CONFIG0	MEM_CONFIG1	MEM_CONFIG2	MEM_CONFIG3	MEM_CONFIG4
Micron 4G/1866	SA00009XU1L	SA00009XU1L	SA00009XU1L	SA00009XU1L		RH51 M4G_1866@ SD028100280 10K_0402_5%	RH54 M4G_1866@ SD028100280 10K_0402_5%	RH56 M4G_1866@ SD028100280 10K_0402_5%	RH57 M4G_1866@ SD028100280 10K_0402_5%	RH60 M4G_1866@ SD028100280 10K_0402_5%
Micron 8G/1866	SA00009U71L	SA00009U71L	SA00009U71L	SA00009U71L		RH52 M8G_1866@ SD028100280 10K_0402_5%	RH53 M8G_1866@ SD028100280 10K_0402_5%	RH56 M8G_1866@ SD028100280 10K_0402_5%	RH57 M8G_1866@ SD028100280 10K_0402_5%	RH60 M8G_1866@ SD028100280 10K_0402_5%
Micron 16G/1866	SA00009ZNL	SA00009ZNL	SA00009ZNL	SA00009ZNL		RH51 M16G_1866@ SD028100280 10K_0402_5%-D	RH53 M16G_1866@ SD028100280 10K_0402_5%-D	RH56 M16G_1866@ SD028100280 10K_0402_5%-D	RH57 M16G_1866@ SD028100280 10K_0402_5%-D	RH60 M16G_1866@ SD028100280 10K_0402_5%-D
Hynix 4G/1866	SA00008G64L H9CCNN8GTALAR-NUD	SA00008G64L H9CCNN8GTALAR-NUD	SA00008G64L H9CCNN8GTALAR-NUD	SA00008G64L H9CCNN8GTALAR-NUD		RH52 H4G_1866@ SD028100280 10K_0402_5%-D	RH54 H4G_1866@ SD028100280 10K_0402_5%-D	RH55 H4G_1866@ SD028100280 10K_0402_5%-D	RH57 H4G_1866@ SD028100280 10K_0402_5%-D	RH60 H4G_1866@ SD028100280 10K_0402_5%-D
Hynix 8G/1866	SA00008FJ4L H9CCNN8BTALAR-NUD	SA00008FJ4L H9CCNN8BTALAR-NUD	SA00008FJ4L H9CCNN8BTALAR-NUD	SA00008FJ4L H9CCNN8BTALAR-NUD		RH51 H8G_1866@ SD028100280 10K_0402_5%-D	RH54 H8G_1866@ SD028100280 10K_0402_5%-D	RH55 H8G_1866@ SD028100280 10K_0402_5%-D	RH57 H8G_1866@ SD028100280 10K_0402_5%-D	RH60 H8G_1866@ SD028100280 10K_0402_5%-D
Hynix 16G/1866	SA0000AENL H9CCNN8LGLAR-NUD	SA0000AENL H9CCNN8LGLAR-NUD	SA0000AENL H9CCNN8LGLAR-NUD	SA0000AENL H9CCNN8LGLAR-NUD		RH52 H16G_1866@ SD028100280 10K_0402_5%-D	RH53 H16G_1866@ SD028100280 10K_0402_5%-D	RH55 H16G_1866@ SD028100280 10K_0402_5%-D	RH57 H16G_1866@ SD028100280 10K_0402_5%-D	RH60 H16G_1866@ SD028100280 10K_0402_5%-D

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				Sheet 3 of 61

Board ID Table for AD channel

RE194	CE75	REV
240K	4700p	X00
130K	4700p	X01
62K	4700p	X02
33K	4700p	X03
8.2K	4700p	A00
4.3K	4700p	
2K	4700p	
1K	4700p	

CPU	4+2	2+3	3+2
Italia CAZ60			

BOARD_ID rise ti ne is measu redfro m5 %68 %

SMBUS Control Table

	SOURCE	BATTERY Charger	PD1	PD2	PWR_MON	5105	XDP	Audio AMP	eDP	Touch Pad	Touch S	IR_THER_S
SMB00_CLK SMB00_DATA	MECS105			V								
SMB01_CLK SMB01_DATA	MECS105											V
SMB02_CLK SMB02_DATA	MECS105									V		
SMB04_CLK SMB04_DATA	MECS105		V									
SMB05_CLK SMB05_DATA	MECS105							V				
SMB07_CLK SMB07_DATA	MECS105				V							
SMB10_CLK SMB10_DATA	MECS105	V										
PCH_SML1CLK PCH_SML1DATA	PCH				V							
SMBCLK SMBDATA	PCH						V					
I2C0_CLK I2C0_DATA	PCH										V	
I2C1_CLK I2C1_DATA	PCH									V		
I2C2_CLK I2C2_DATA	PCH								V			

CLK	DIFFERENTIAL CLK#	DESTINATION	PCI EXPRESS PORT#	DESTINATION
	CLKOUT_PCIE0	Alpine Ridge	Lane 1	Card Reader
	CLKOUT_PCIE1	NGFF WLAN	Lane 2	NC
	CLKOUT_PCIE2	NC	Lane 3	NGFF WLAN
	CLKOUT_PCIE3	M.2 SSD	Lane 4	NC
	CLKOUT_PCIE4	NC	Lane 5	Alpine Ridge
	CLKOUT_PCIE5	Card Reader	Lane 6	Alpine Ridge
	FLEX CLK#	DESTINATION	Lane 7	Alpine Ridge
	CLKOUT_LPC_0	ESPI 5105	Lane 8	Alpine Ridge
	CLKOUT_LPC_1	NC	Lane 9	M.2 SSD
			Lane 10	M.2 SSD
			Lane 11	M.2 SSD
			Lane 12 / SATA 2	M.2 SSD

SATA PORT#	DESTINATION
SATA-0	NC
SATA-1A	NC
SATA-1B	NC
SATA-2	M.2 SSD

PCH USB 2.0 Port Mapping	USB PORT#	DESTINATION
	1	PD PORT3
	2	NC
	3	NC
	4	NC
	5	IR Camera & Cam
	6	NC
	7	NGFF WLAN BT
	8	NC
	9	NC
	10	Fingerprint
PCH USB 3.0 Port Mapping	1	DP MX (PS8743B)
	2	
PCH DDI Port Mapping	DDI PORT#	DESTINATION
	1	Alpine Ridge
	2	Alpine Ridge

Symbol Note :

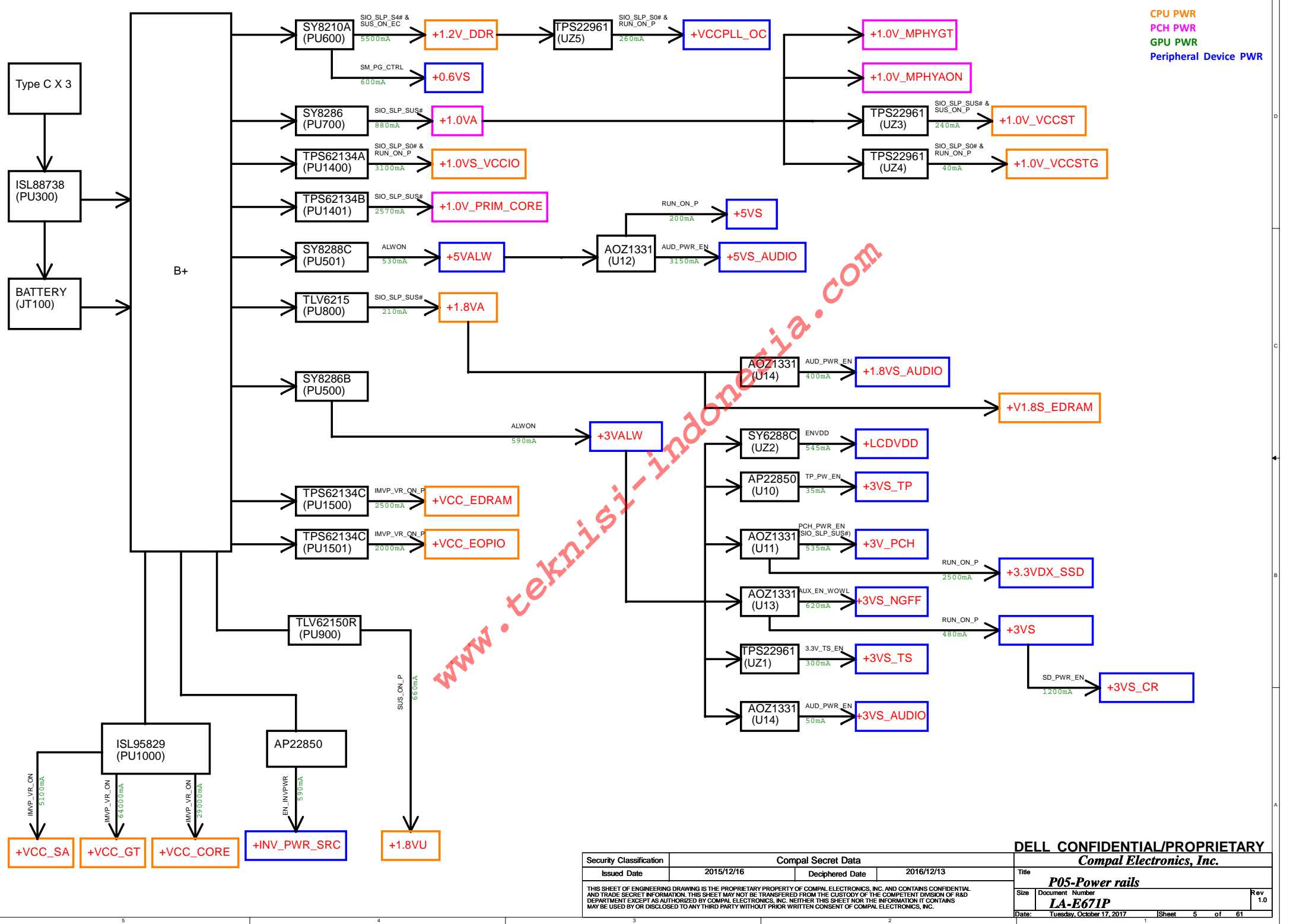


: means Digital Ground



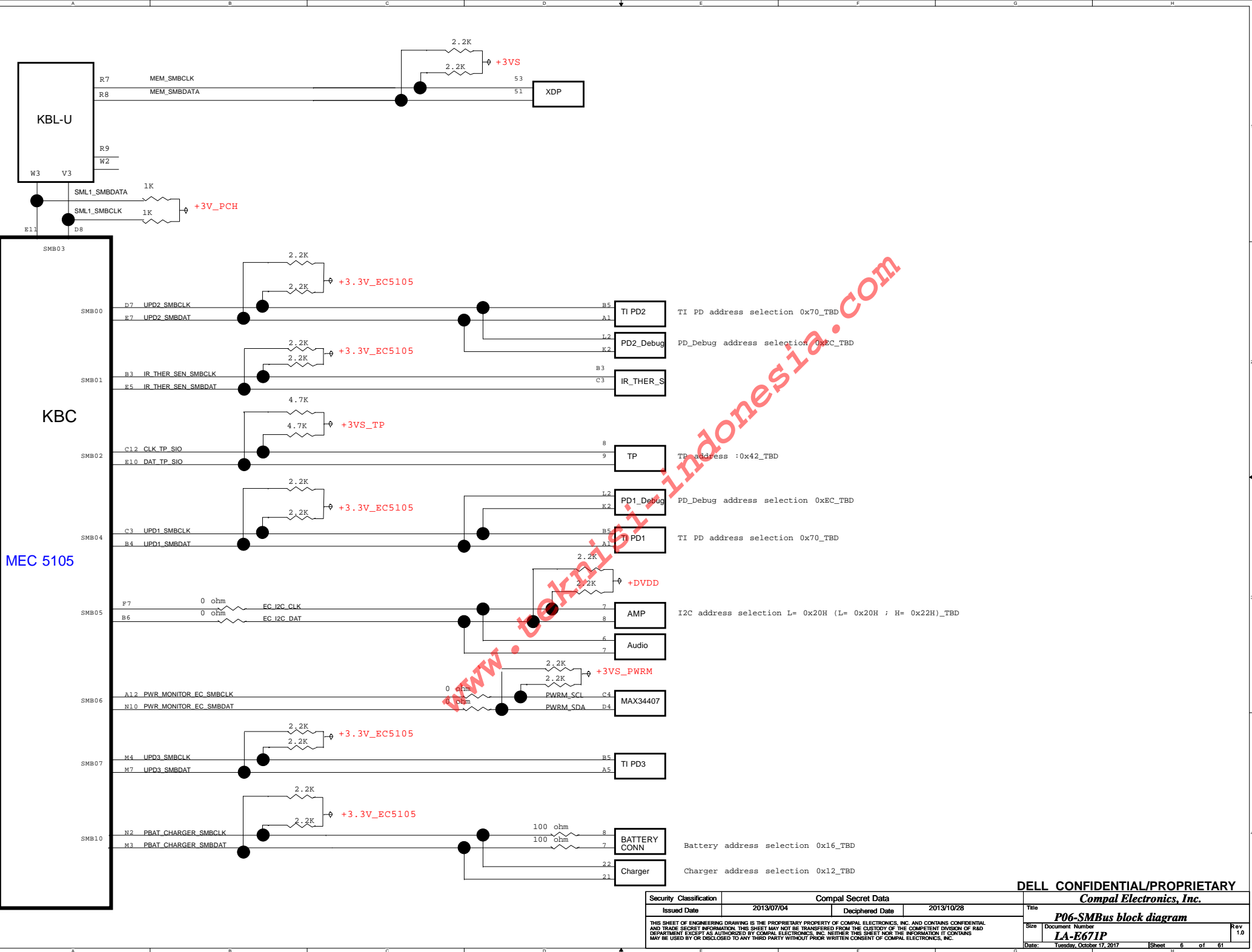
: means Analog Ground

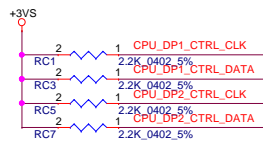
Security Classification				Compal Secret Data				DELL CONFIDENTIAL/PROPRIETARY			
Issued Date				2015/12/16				Compal Electronics, Inc.			
Deciphered Date				2016/12/13				P04-Notes List			
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								LA-E671P			
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								Sheet 4 of 61			



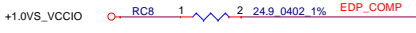
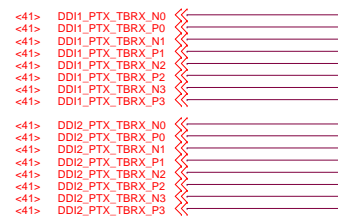
CPU PWR
PCH PWR
GPU PWR
Peripheral Device PWR

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Issued Date		Deciphered Date		Compal Electronics, Inc.	
2015/12/16		2016/12/13		Title	
				P05-Power rails	
				Size Document Number	
				LA-E671P	
				Rev 1.0	
				Date: Tuesday, October 17, 2017	
				Sheet 5 of 61	





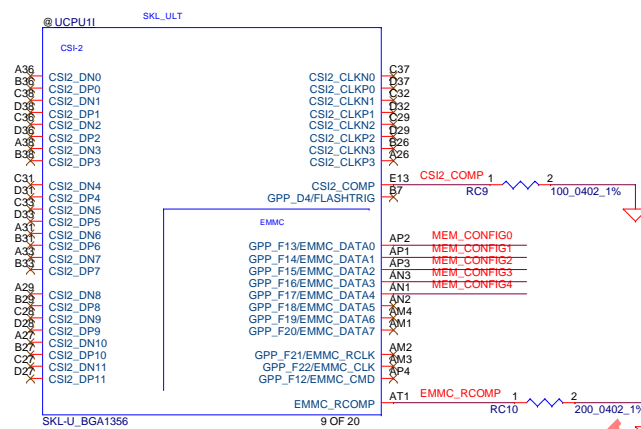
Alpine Ridge



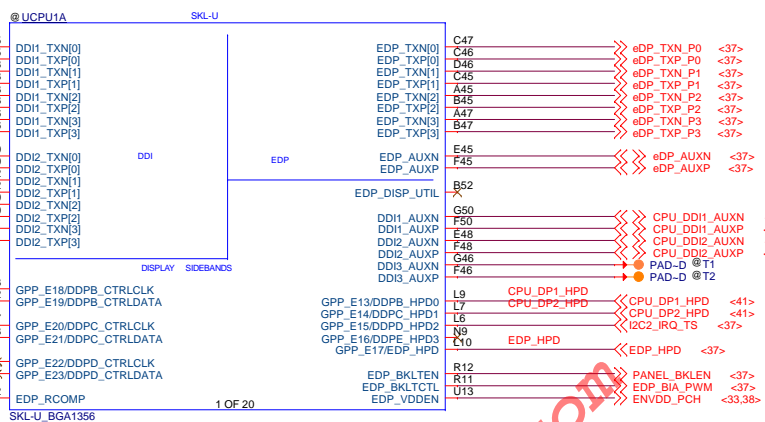
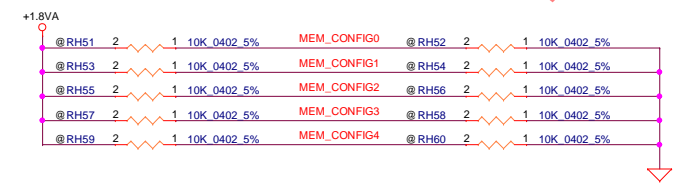
COMPENSATION PU FOR EDP

CAD Note: Trace width=5 mils, Isolat i on Spad ng=25 m, Max length=600 mils.

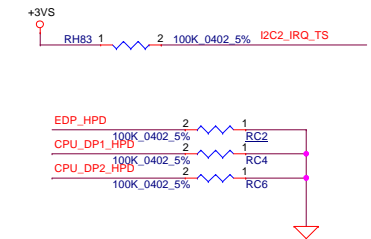
SKL-U Ballout Rev0.71 & INTEL symbol Rev1.0



DDR Memory Configurati no Type Strap ph



Support QHD



GPIO Pin	Pin Name		1600 Mbps								
			Micron 4G	Micron 8G	Micron 16G	Hynix 4G	Hynix 8G	Hynix 16G	Samsung 4G	Samsung 8G	Samsung 16G
GPP_F13	MEM_CONFIG0		0	1	0	1	0	1	0	1	0
GPP_F14	MEM_CONFIG1		0	0	1	1	0	0	1	1	0
GPP_F15	MEM_CONFIG2		0	0	0	0	1	1	1	1	0
GPP_F16	MEM_CONFIG3		0	0	0	0	0	0	0	0	1
GPP_F17	MEM_CONFIG4		0	0	0	0	0	0	0	0	0

GPIO Pin	Pin Name		1866 Mbps								
			Micron 4G	Micron 8G	Micron 16G	Hynix 4G	Hynix 8G	Hynix 16G	Samsung 4G	Samsung 8G	Samsung 16G
GPP_F13	MEM_CONFIG0		1	0	1	0	1	0	1	0	1
GPP_F14	MEM_CONFIG1		0	1	1	0	0	1	1	0	0
GPP_F15	MEM_CONFIG2		0	0	0	1	1	1	1	0	0
GPP_F16	MEM_CONFIG3		1	1	1	1	1	1	1	0	0
GPP_F17	MEM_CONFIG4		0	0	0	0	0	0	0	1	1

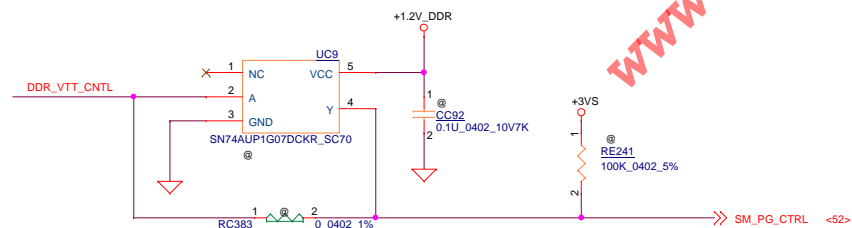
GPIO Pin	Pin Name		2133 Mbps								
			Micron 4G	Micron 8G	Micron 16G	Hynix 4G	Hynix 8G	Hynix 16G	Samsung 4G	Samsung 8G	Samsung 16G
GPP_F13	MEM_CONFIG0		0	1	0	1	0	1	0	1	0
GPP_F14	MEM_CONFIG1		1	1	0	0	1	1	0	0	1
GPP_F15	MEM_CONFIG2		0	0	1	1	1	1	0	0	0
GPP_F16	MEM_CONFIG3		0	0	0	0	0	0	1	1	1
GPP_F17	MEM_CONFIG4		1	1	1	1	1	1	1	1	1

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Title		P07-MCP(1/14)DD1,EDP,CSI2,EMMC	
Size	Document Number	LA-E671P	
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LPDDR3, Ballout for side by side(Non-Interleave)

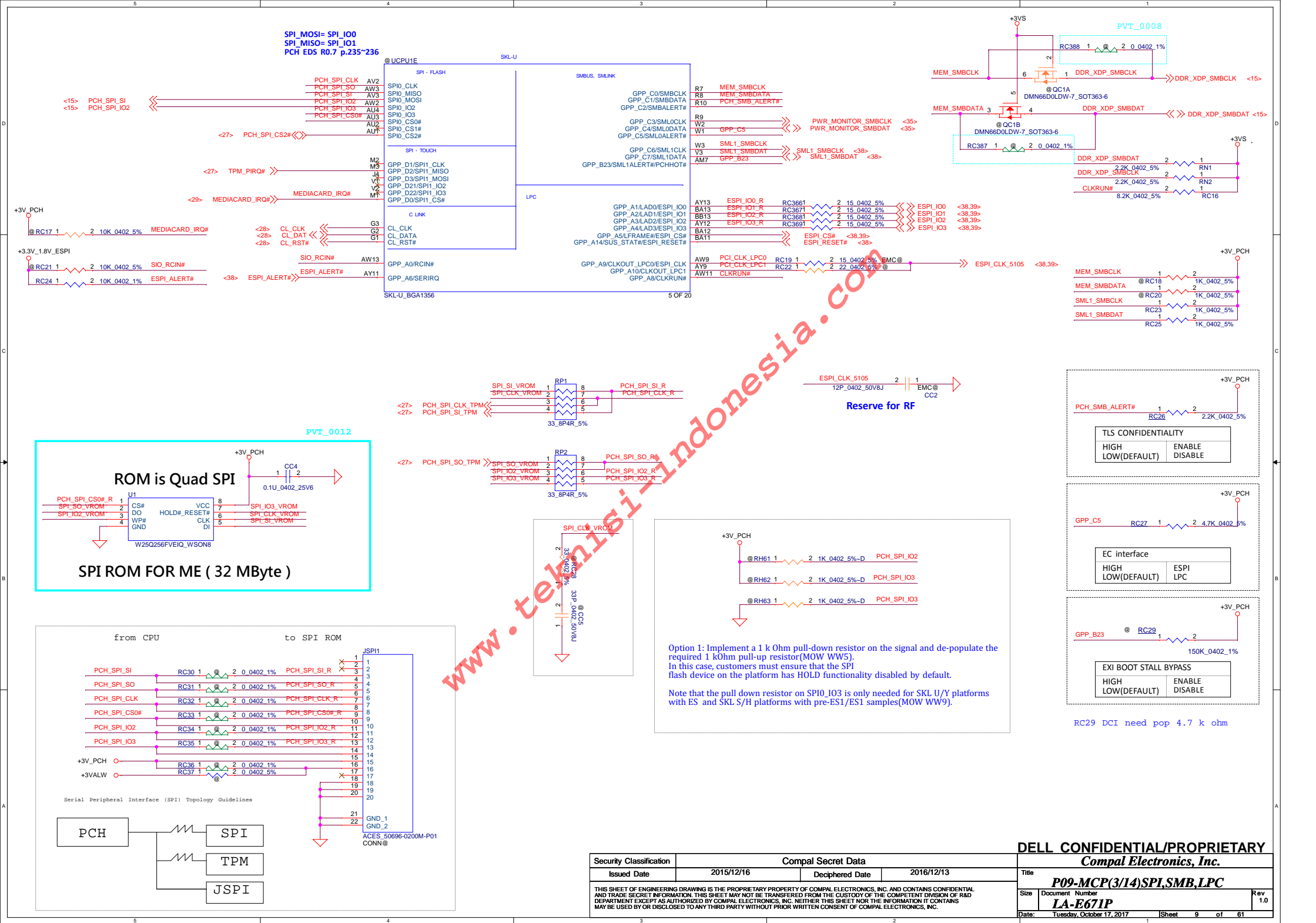


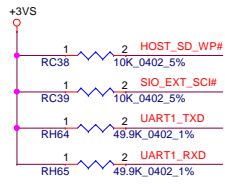
LPDDR3 COMPENSATION SIGNALS



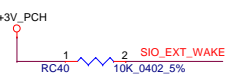
CAD Note:
Trace width=12~15 mil, Spacing=20 mils
Max trace length= 500 mil

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					LA-E671P
				Date:	Tuesday, October 17, 2017
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				Rev	0.1

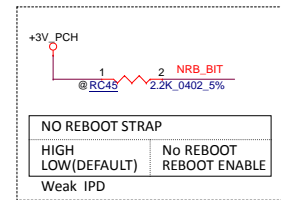
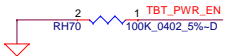




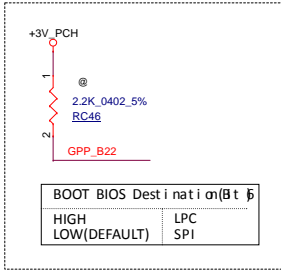
change to net name ==> I2C0_SDA_TS and I2C0_SCK_TS



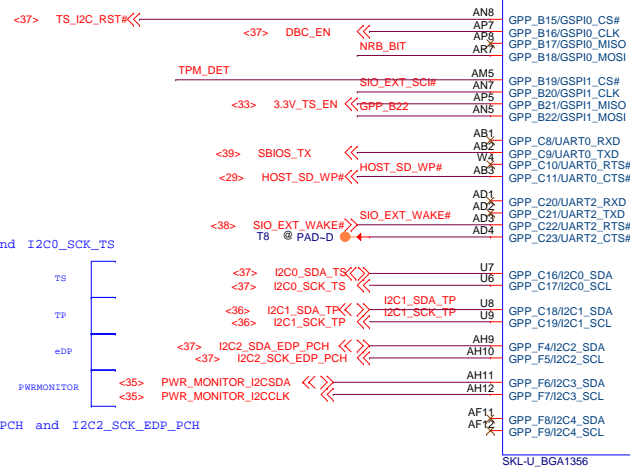
change to net name ==> I2C2_SDA_EDP_PCH and I2C2_SCK_EDP_PCH



NO REBOOT STRAP	
HIGH	No REBOOT
LOW(DEFAULT)	REBOOT ENABLE
Weak IPD	

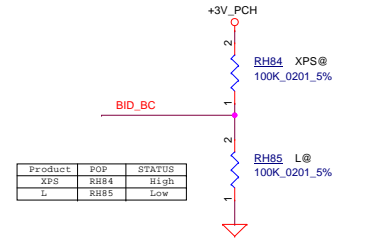
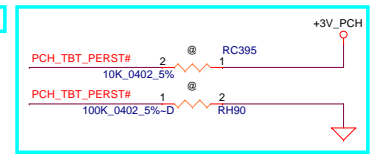
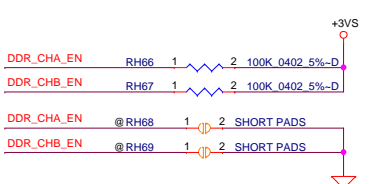
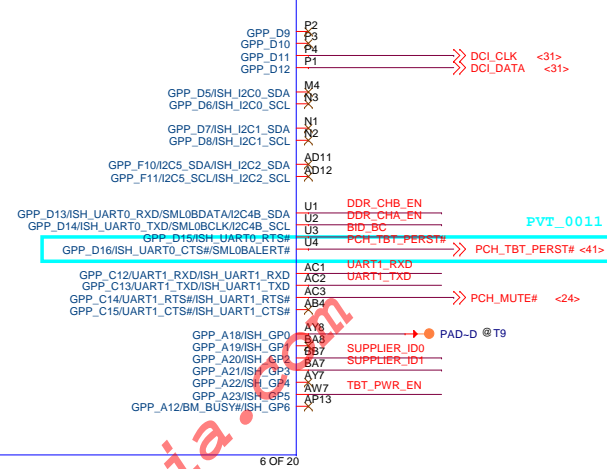
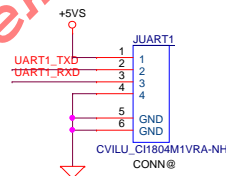


BOOT BIOS Destination(Bt p	
HIGH	LPC
LOW(DEFAULT)	SPI

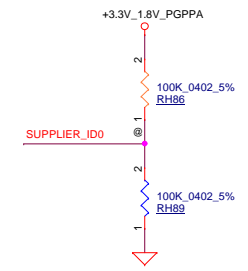
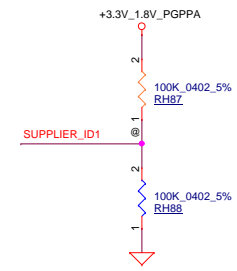


TPM BOM Optional

TPM_DET	
TPM	1 = W/TPM
	0 = W/O TPM



Product	POP	STATUS
XPS	RH84	High
L	RH85	Low



RH87	RH88	RH86	RH89	REV
V	V	V	V	0 0
V	V	V	V	0 1
V	V	V	V	1 0
V	V	V	V	1 1

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Title	P10-MCP(4/14)GSPI,I2C,UART,ISH	
Size	Document Number	Rev
	LA-E671P	1.0
Date:	Tuesday, October 17, 2017	Sheet 10 of 61

Cardreader
PCIe Gen2 x 1

<29> PCIE_PRX_CARDTX_N1
<29> PCIE_PRX_CARDTX_P1
<29> PCIE_PTX_CARDRX_N1
<29> PCIE_PTX_CARDRX_P1

WLAN
PCIe Gen2 x 1

<28> PCIE_PRX_WLANTX_N3
<28> PCIE_PRX_WLANTX_P3
<28> PCIE_PTX_WLANRX_N3
<28> PCIE_PTX_WLANRX_P3

Alpine Ridge
PCIe Gen3 x 4

<41> PCIE_PRX_TBTX_N5
<41> PCIE_PRX_TBTX_P5
<41> PCIE_PTX_TBRX_N5
<41> PCIE_PTX_TBRX_P5

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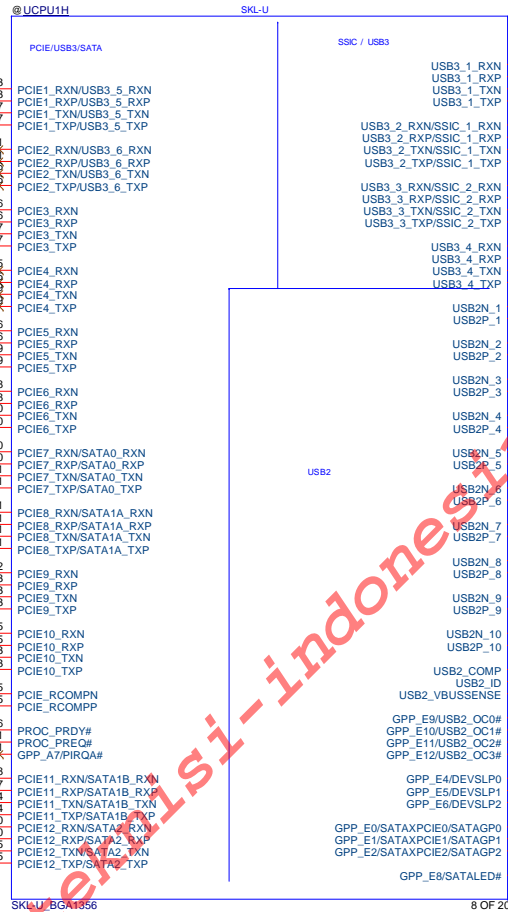
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M.2 SSD
PCIe Gen3 x 4

PCIE_RCOMP_N
PCIE_RCOMP_P
CPU_XDP_PRDY#
CPU_XDP_FREQ#

SATA SSD

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<30> PCIE_PRX_SSDTX_P11
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<30> SATA_PTX_SSDRX_P2



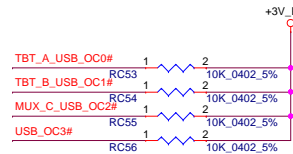
USB3.0 DP MX (PS8743B)

USB2.0 for USB PD PORT3

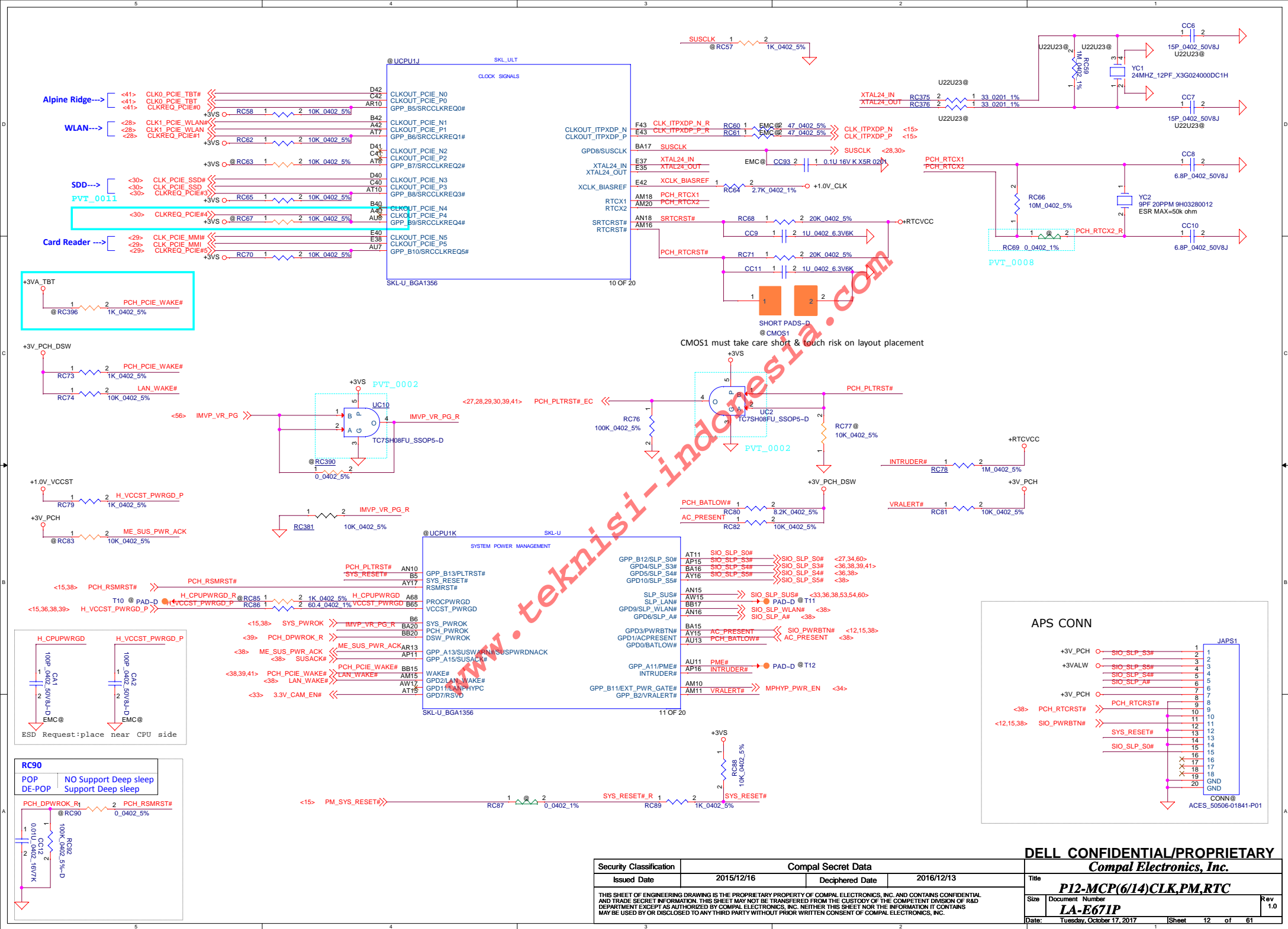
CAM & IR CAM

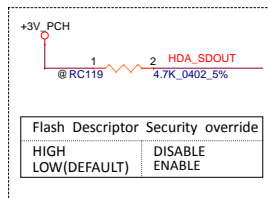
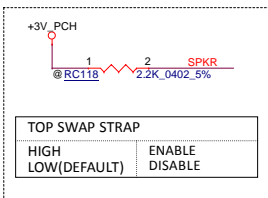
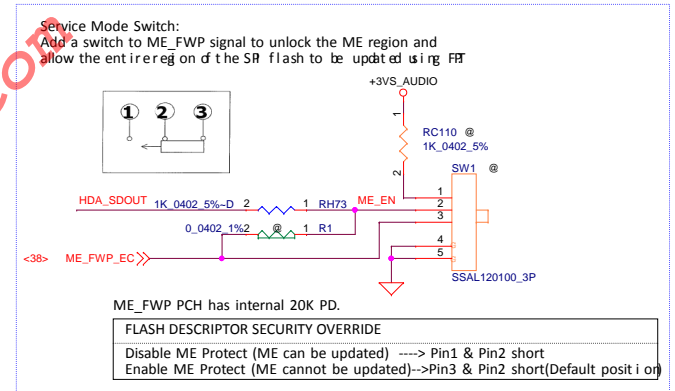
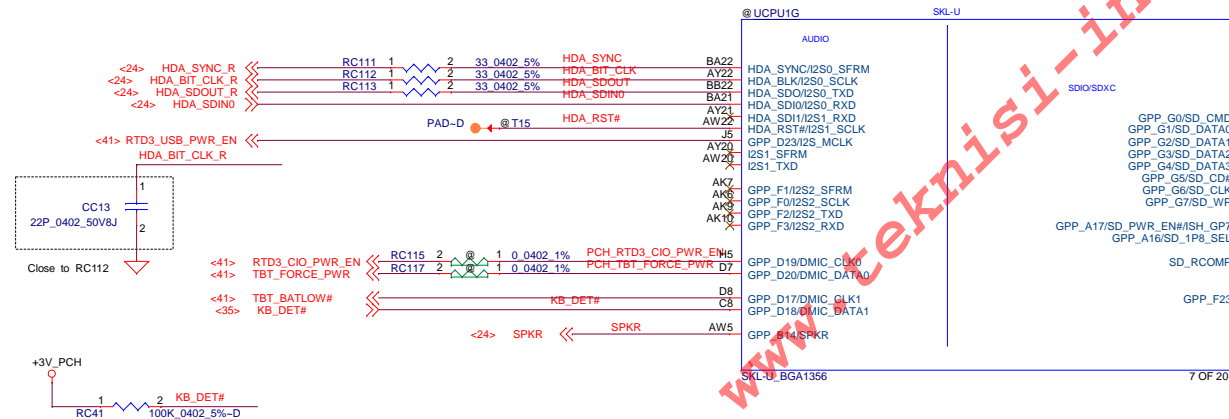
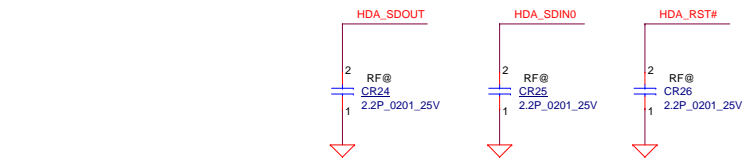
NGFF (WLAN)

Fingerprint



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Issued Date				2015/12/16	Deciphered Date	2016/12/13	Title
							Compal Electronics, Inc.
							P11-MCP(5/14)PCIE,USB,SATA
							LA-E671P
							Rev 1.0
							Date: Tuesday, October 17, 2017
							Sheet 11 of 61





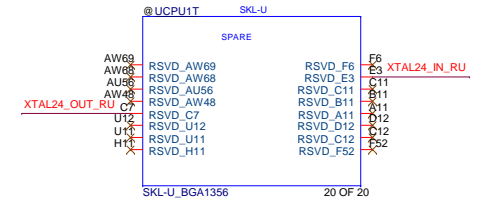
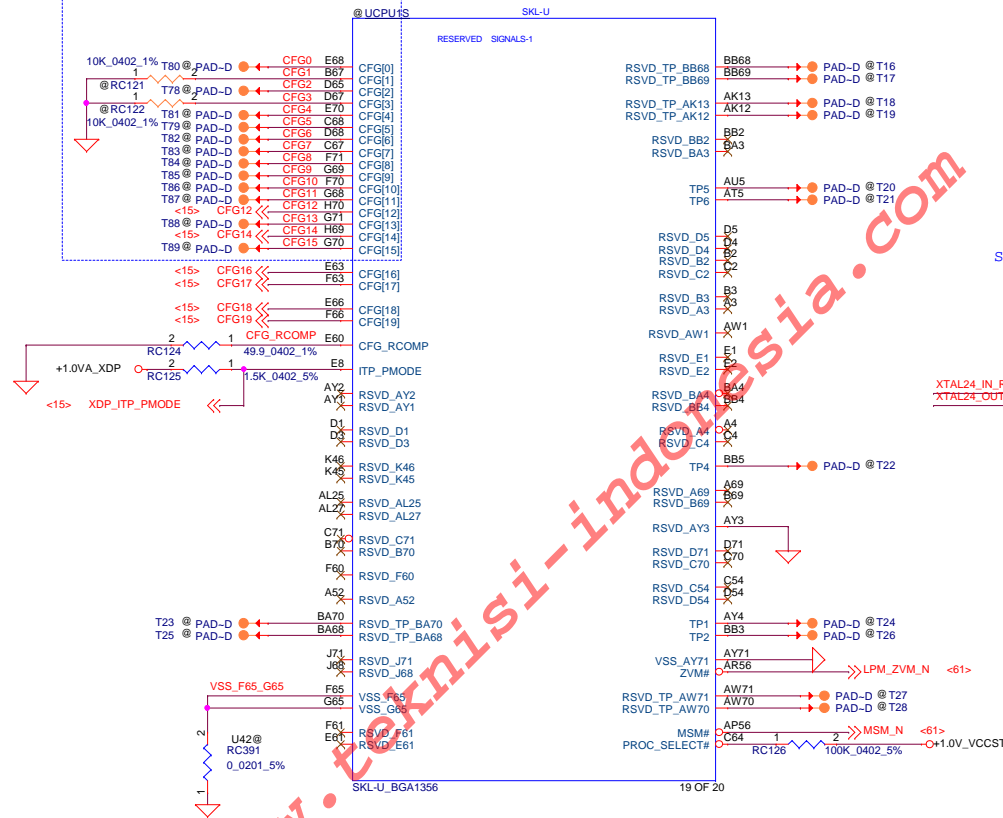
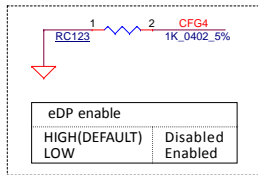
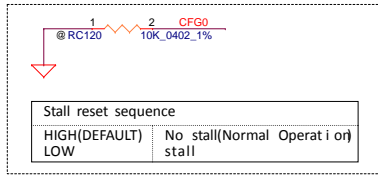
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Deciphered Date		2016/12/13		Title	
				P13-MCP(7/14)MISC,JTAG,HDA,SDIO	
				Size Document Number	
				LA-E671P	
				Rev 1.0	
				Date: Tuesday, October 17, 2017	
				Sheet 13 of 61	

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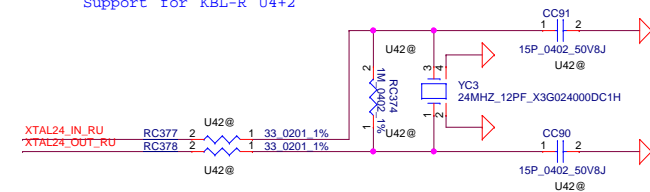
<15> CFGQ[0..15] <<

● UCPU15

10K_0402_1% T80 @ PAD-D-1 ● CFG0 E68 CFGQ[0]
 1 T78 @ PAD-D-2 ● CFG2 D65 CFGQ[1]
 @RC121 1 T78 @ PAD-D-3 ● CFG3 D67 CFGQ[2]
 10K_0402_1% T81 @ PAD-D-4 ● CFG4 E70 CFGQ[3]
 T79 @ PAD-D-5 ● CFG5 C88 CFGQ[4]
 T82 @ PAD-D-6 ● CFG6 D88 CFGQ[5]
 T83 @ PAD-D-7 ● CFG7 C67 CFGQ[6]
 T84 @ PAD-D-8 ● CFG8 F71 CFGQ[7]
 T85 @ PAD-D-9 ● CFG9 G69 CFGQ[8]
 T86 @ PAD-D-10 ● CFG11 G68 CFGQ[9]
 T87 @ PAD-D-11 ● CFG12 H70 CFGQ[10]
 <15> CFG12 H70 CFGQ[11]
 T88 @ PAD-D-12 ● CFG13 G71 CFGQ[12]
 <15> CFG14 H69 CFGQ[13]
 T89 @ PAD-D-13 ● CFG15 G70 CFGQ[14]
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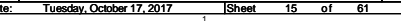
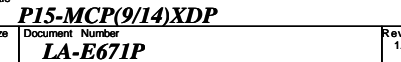
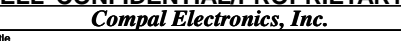
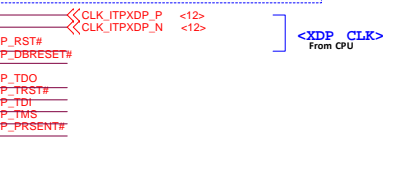
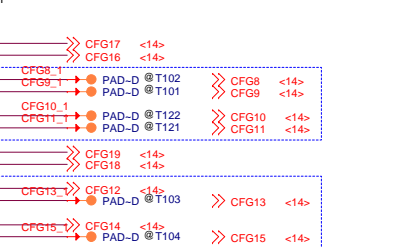
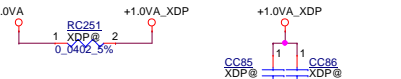
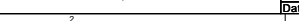
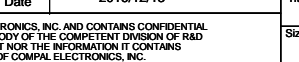
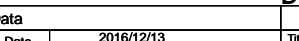
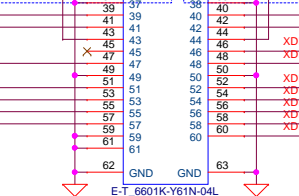
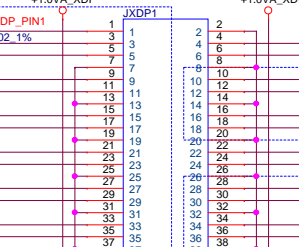
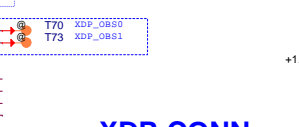
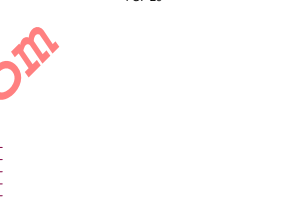
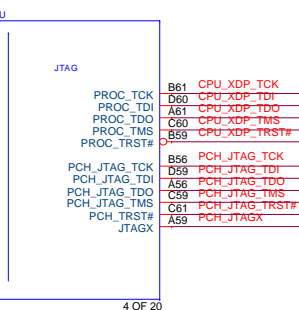
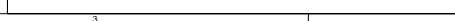
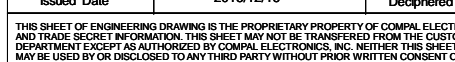
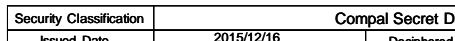
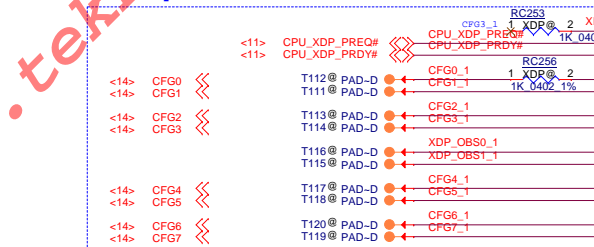
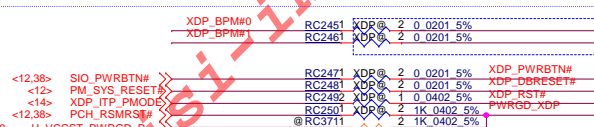
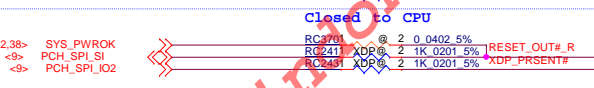
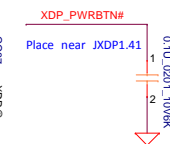
Support for KBL-R U4+2



ZVM# for SKYLAKE-U 2+3e

MSM# for SKYLAKE-U 2+3e

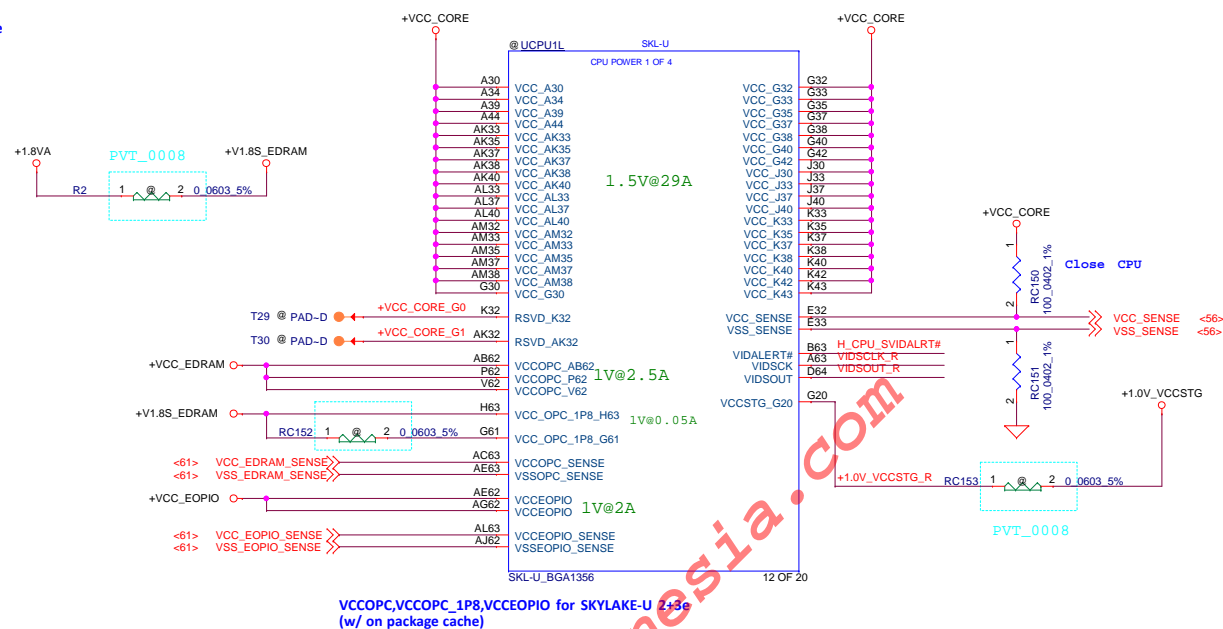
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				P14-MCP(8/14)CFG.RSVD	
				Size	Document Number
				LA-E671P	1.0
				Date: Tuesday, October 17, 2017	Sheet 14 of 61



PSC(Primary side cap) : Place as close to the package as possible
BSC(Backside cap) : Place on secondary side, underneath the package

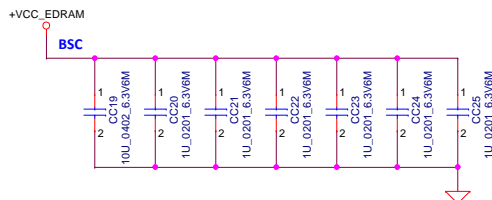
Component placement order:
Package edge > 0402 caps > 0805 caps > Bulk caps > Power source

+VCC_CORE: 0.55~1.5V, 29A
+VCC_EDRAM: 1V, 2.5A
+V1.8S_EDRAM: 1.8V, 50mA
+VCC_EOPIO: 0.8~1V, 2A

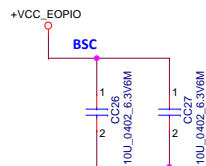


VCCOPC,VCCOPC_1P8,VCCEPIO for SKYLAKE-U 2436
(w/ on package cache)

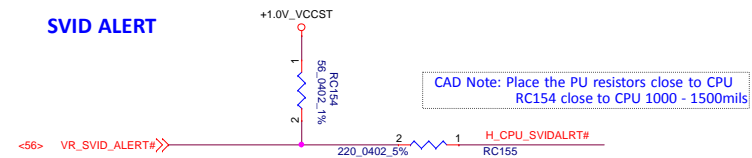
+VCC_EDRAM Decoupling Requirement
Back Side (underneath the package):
10U_0402*1 pcs + 1U_0201*6 pcs



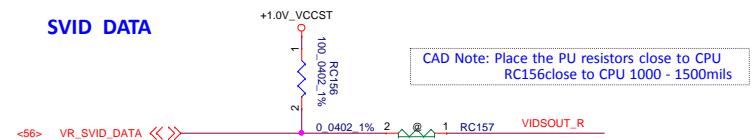
+VCC_EOPIO Decoupling Requirement
Back Side (underneath the package):
10U_0402*2 pcs



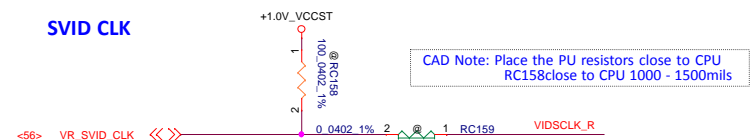
SVID ALERT



SVID DATA

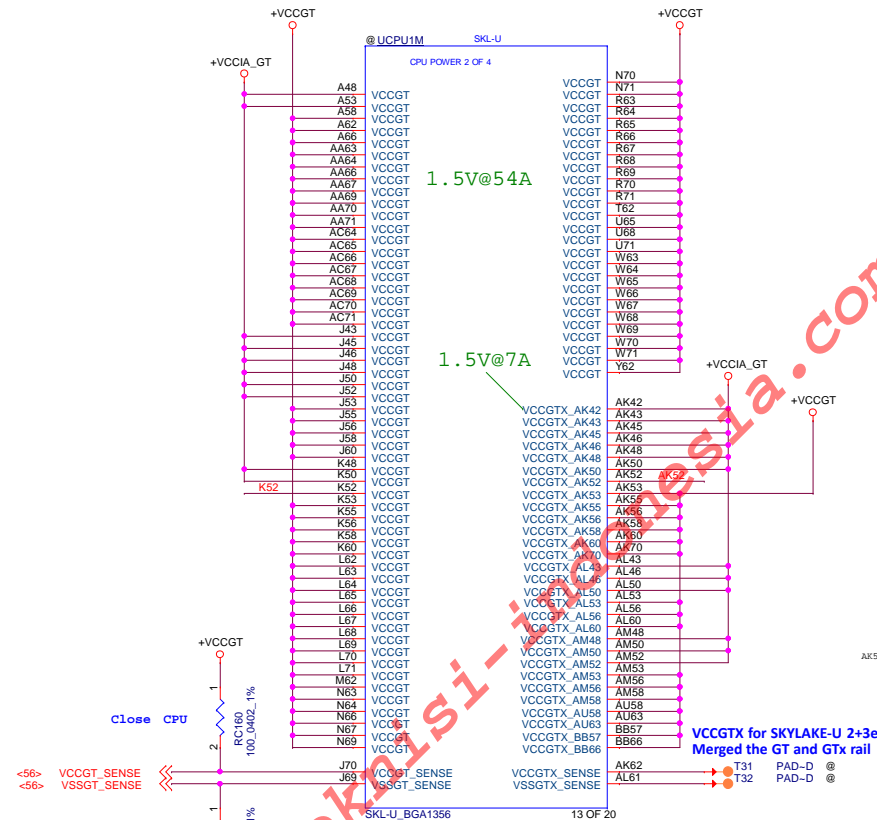


SVID CLK

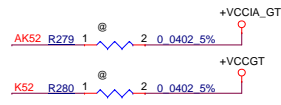
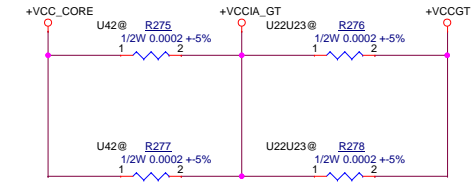


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Issued Date				2015/12/16	Deciphered Date	2016/12/13	Title
							P16-MCP(10/14)PWR-VCC CORE
							Size Document Number
							LA-E671P
							Rev 1.0
							Date: Tuesday, October 17, 2017
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+VCCGT: 0.55~1.5V, 54A
+VCCGTx : 0.55~1.5V, 7A



Note: 4+2 Co-layout Only can use SD00001V200



KBL-R U42 Only Design	Do not Connect AK52 and K52 Balls, Keep as NC
KBL-R U42 Compatible Design for (KBL-R U42/KBL U22/KBL U23e) support	Do not Connect AK52 and K52 Balls, Keep as NC

AK52 and K52 Kaby Lake Silicon Ball Connectivity Recap from PDG (568813_KBL_R_U42_PDG_Addendum_Rev0p9, Page 12)

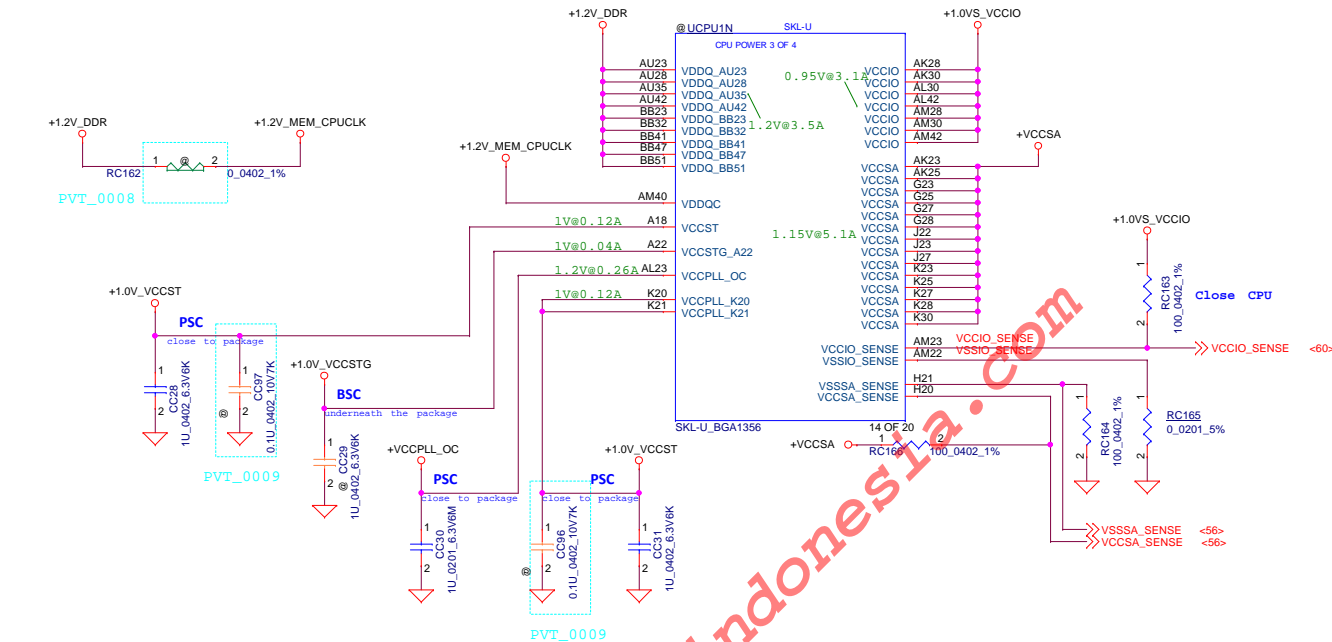
VCCGTx for SKYLAKE-U 2+3e
Merged the GT and GTX rail

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Title	P17-MCP(11/14)PWR-VCCGT	
Size	Document Number	Rev
	LA-E671P	1.0
Date:	Tuesday, October 17, 2017	Sheet 17 of 61

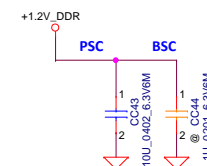
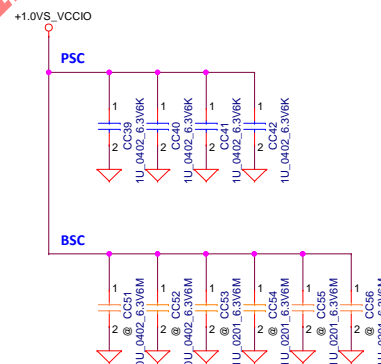
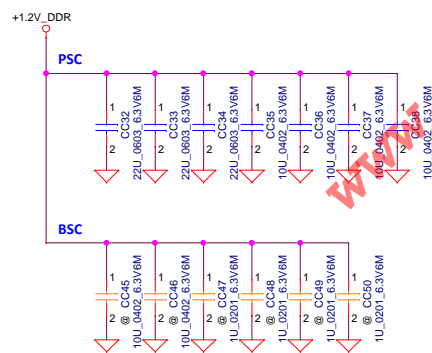
+1.2V_DDR: 1.2V, 3.5A
+1.0V_VCCST: 1V, 120mA; VCCPLL: 1V, 120mA
+1.0V_VCCSTG: 1V, 40mA
+VCCPLL_OC: 1.2V, 260mA
+1.0VS_VCCIO: 0.85~0.95V, 3.1A
+VCC_SA: 1.15V, 5.1A



+1.2_DDR Decoupling Requirement
 Back Side (underneath the package):
 10U_0402*2 pcs + 1U_0201*4 pcs (@)
 Primary Side (close to package):
 10U_0402*4 pcs + 22U_0603*3 pcs

+1.0VS_VCCIO Decoupling Requirement
 Back Side (underneath the package):
 10U_0402*2 pcs + 1U_0201*4 pcs (@)
 Primary Side (close to package):
 10U_0402*4 pcs

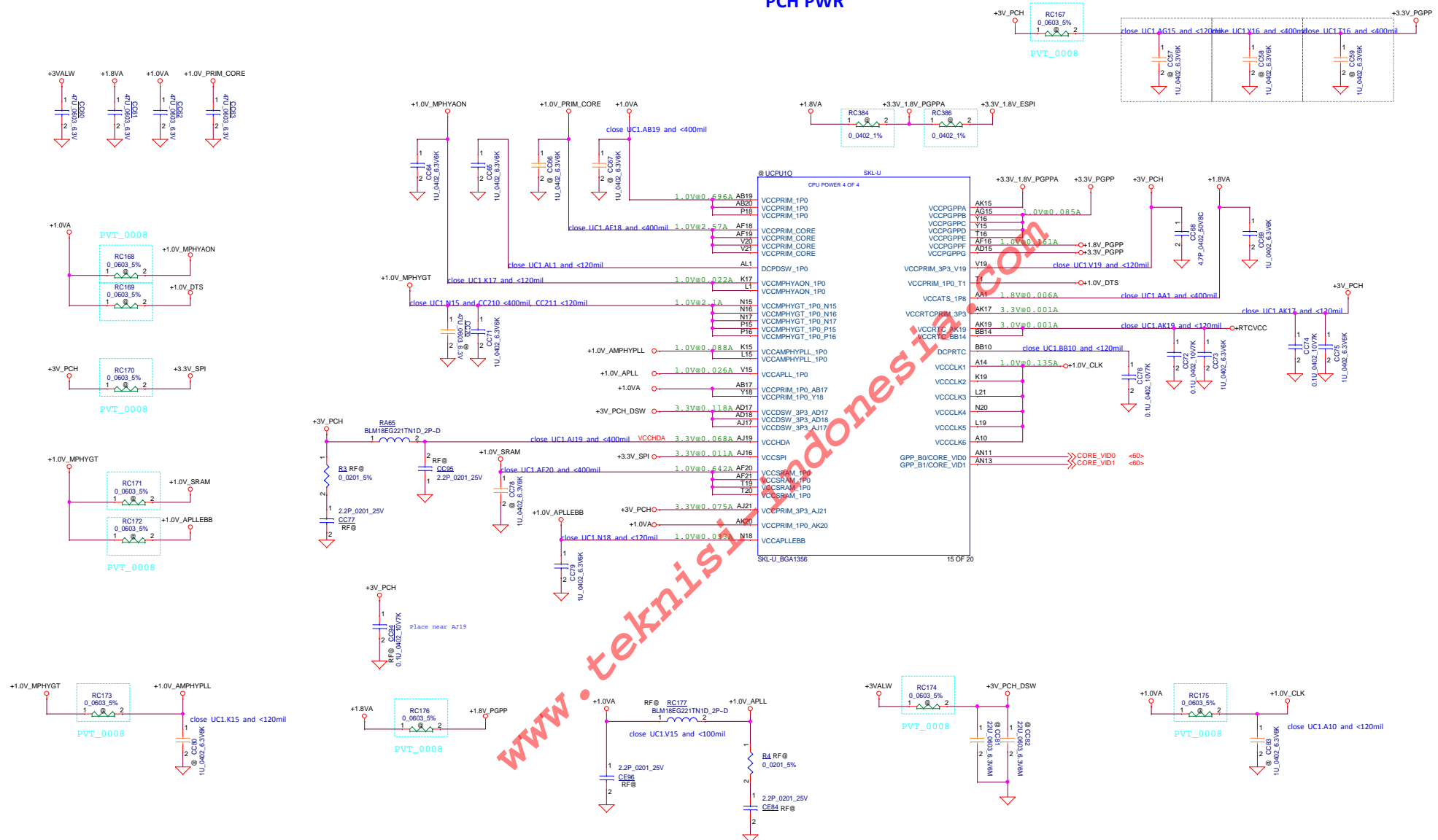
+1.2V_MEM_CPUCLK (VDDQC) Place on CPU
 Back Side (underneath the package):
 1U_0201*1 pcs (@)
 Primary Side (close to package):
 10U_0402 * 1 pcs



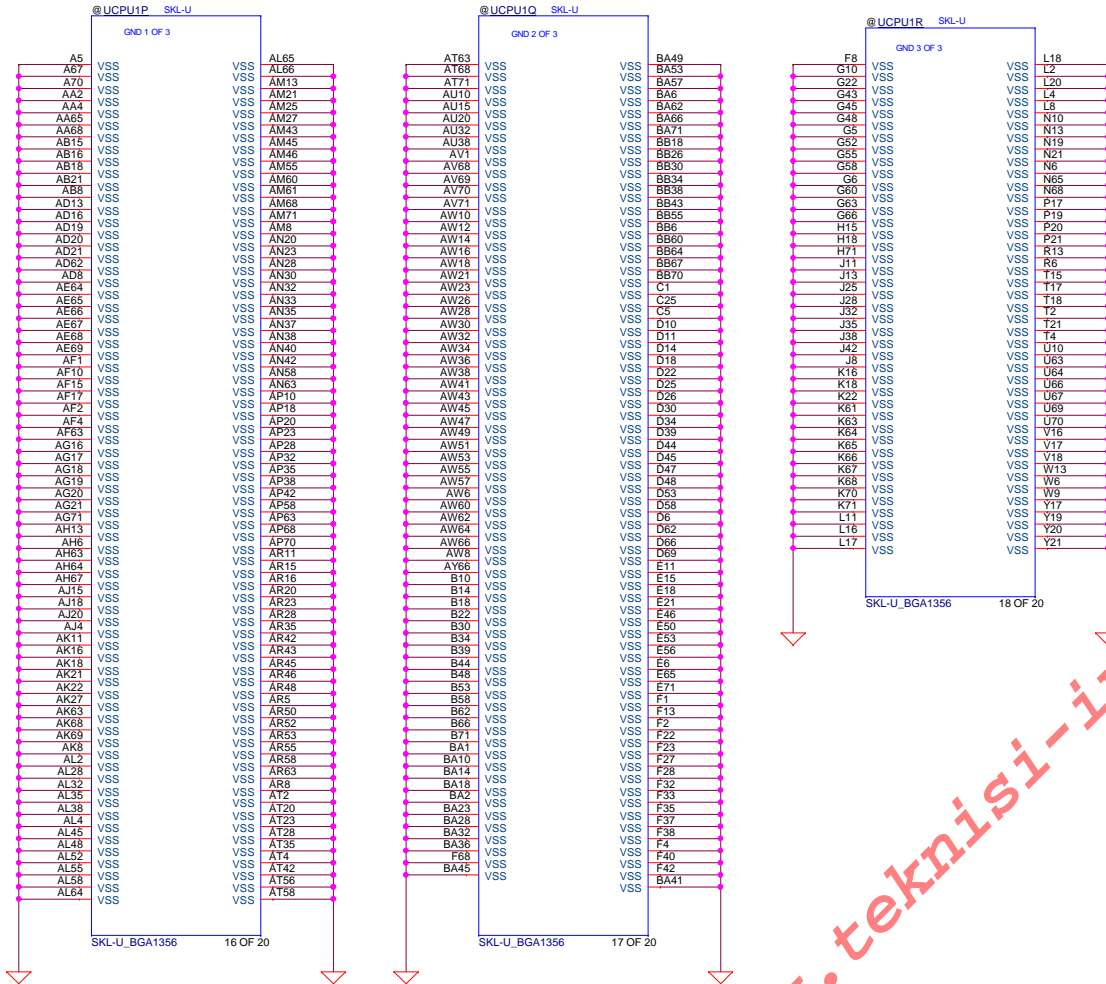
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Compal Electronics, Inc.			
Title	P18-MCP(12/14)PWR-VCCIO.MEM		
Size	Document Number	Rev	1.0
Date:	Tuesday, October 17, 2017	Sheet	18 of 61

PCH PWR

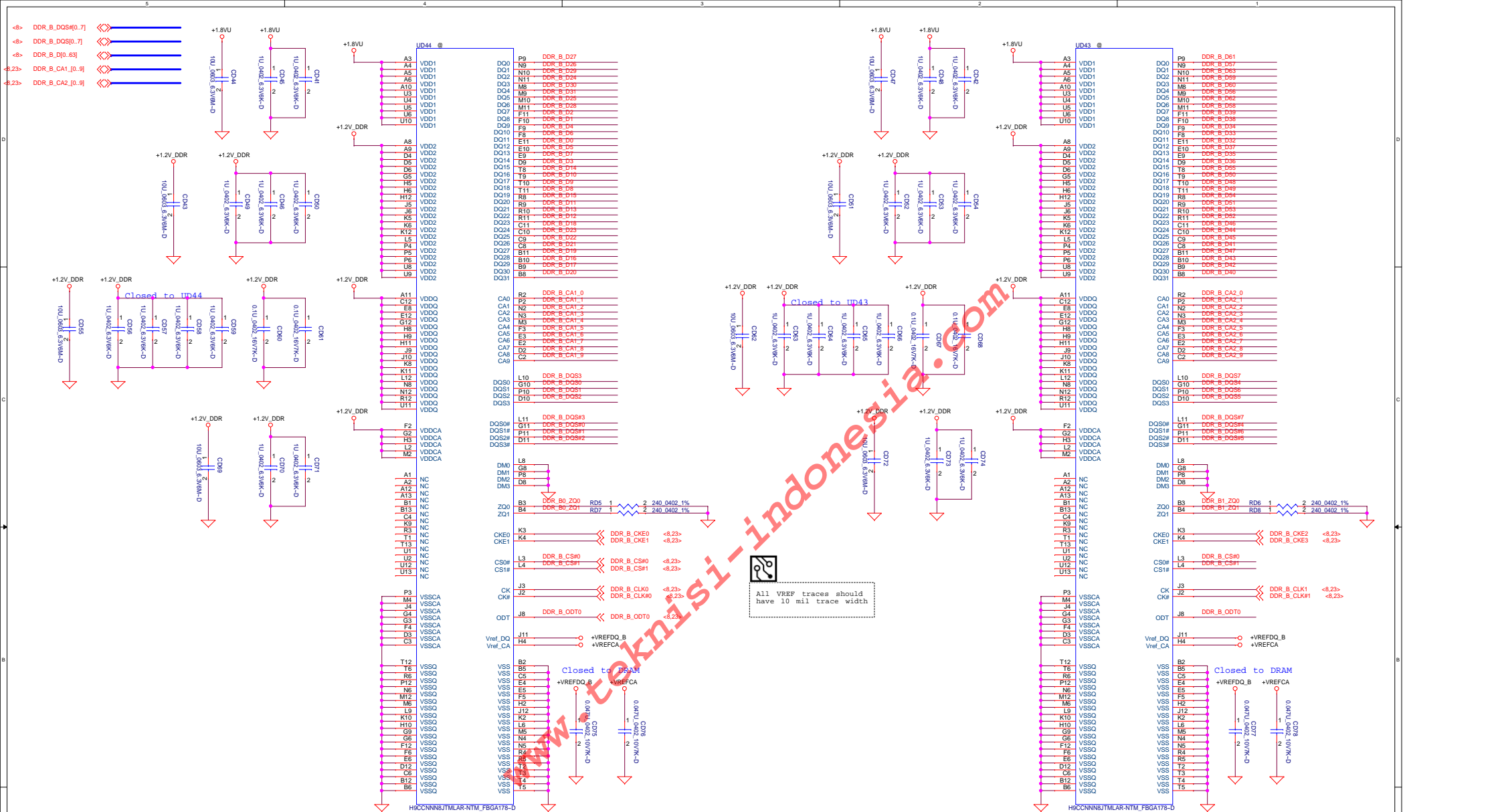
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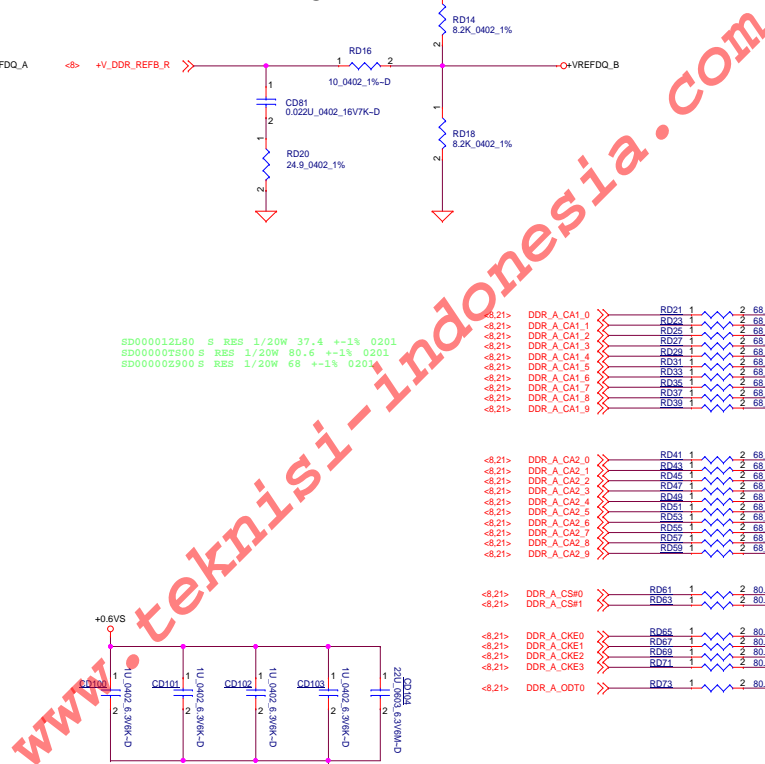
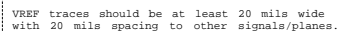
Note1: VCCPRIM_CORE Implementat i on ũt h PCH CORE_V D Reco mnendat i on



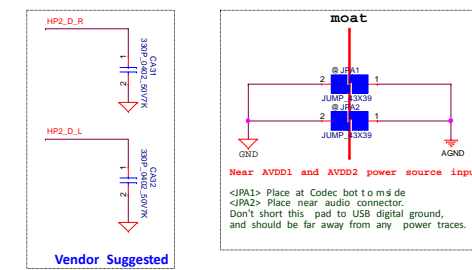
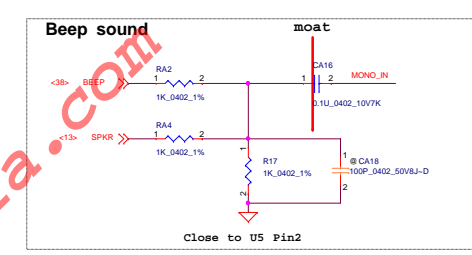
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				P20-MCP(14/14)VSS	
Size		Document Number			Rev
		LA-E671P			1.0
Date:		Tuesday, October 17, 2017		Sheet	20 of 61



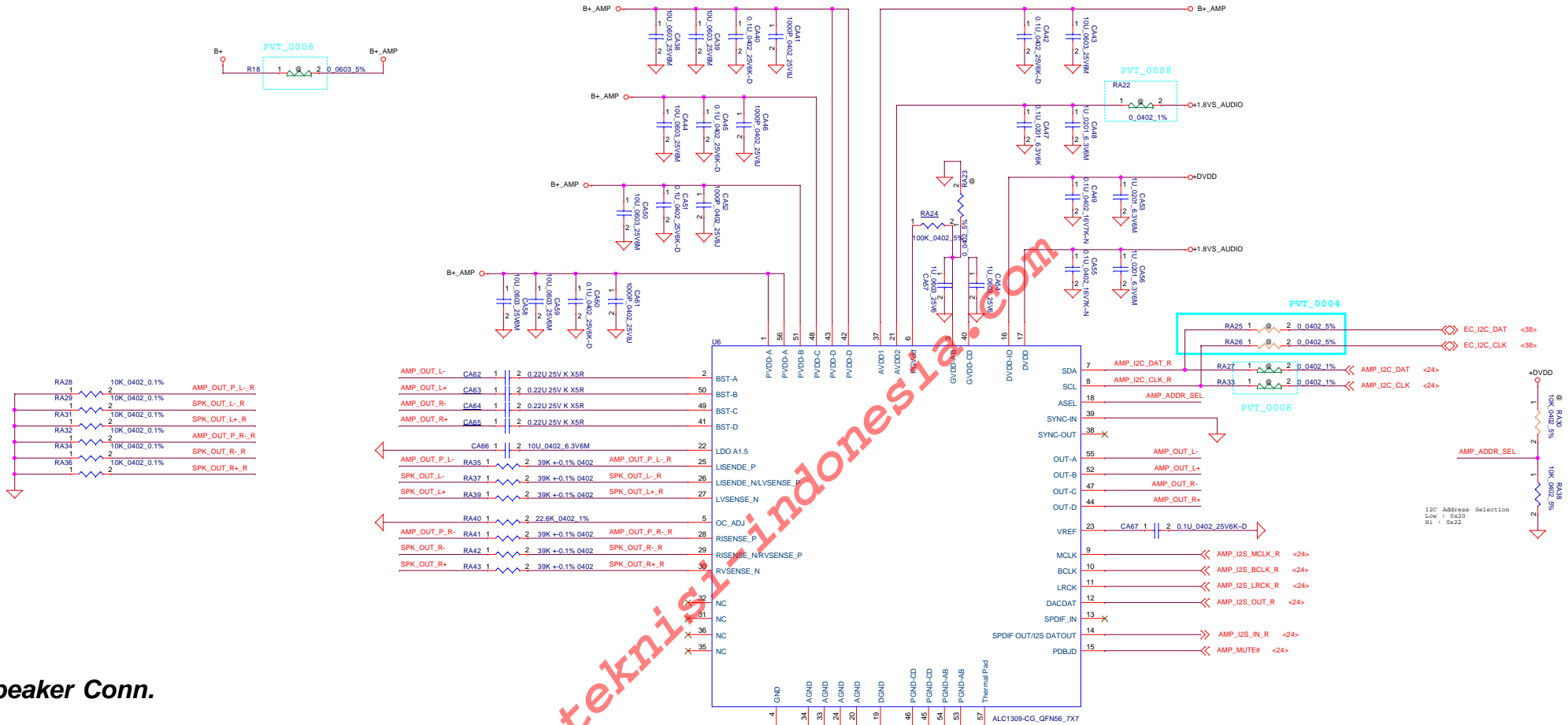


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				Rev 1.0	
				Date:	Tuesday, October 17, 2017
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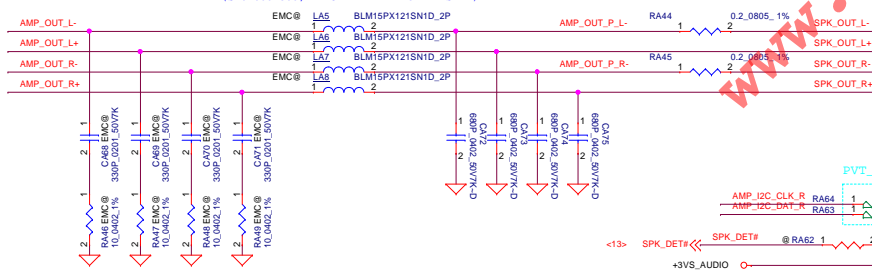
Security Classification		Compal Secret Data		DECLASSIFIED/CONFIDENTIAL Compal Electronics, Inc.	
Issued Date	2013/07/04	Deciphered Date	2013/10/28	Title	P24-Audio Codec3271
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SMART AMP



Int. Speaker Conn.

Use 120 ohm bead (SM01000L300, MURATA) 40mil = For 4ohm 3W Speaker



Function	RA50	RA62
EEPROM Speaker	0 ohm	NC
Speaker Detection	10K	0 ohm

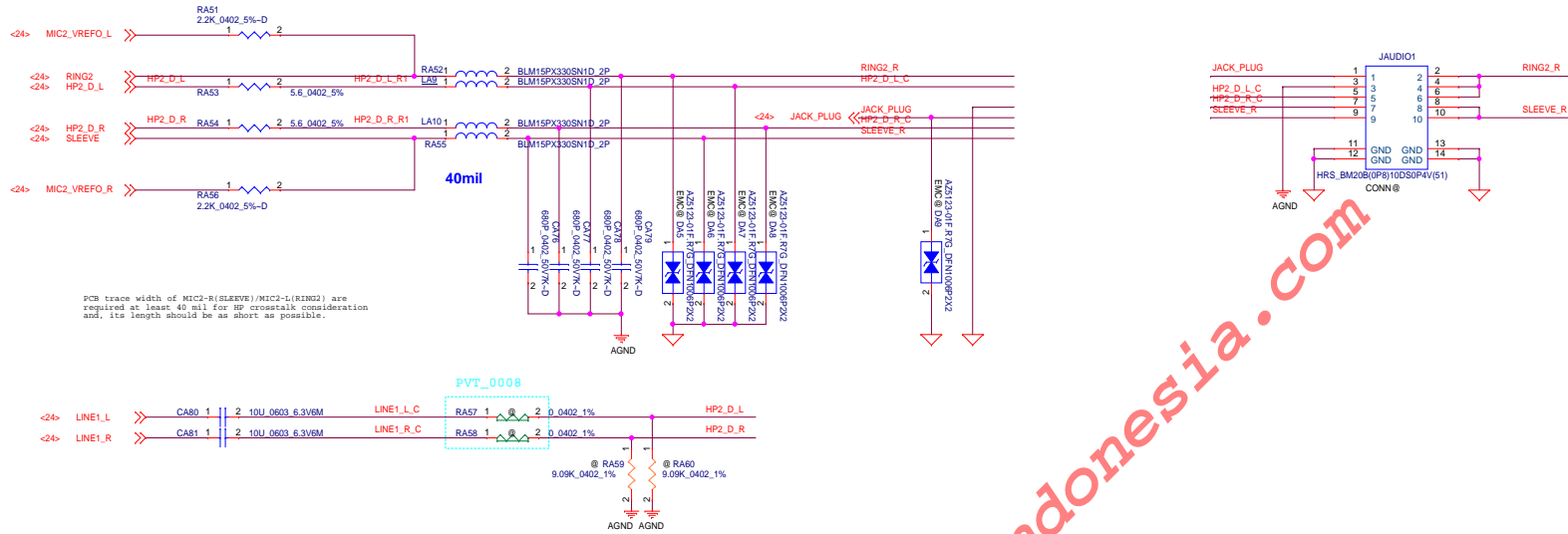
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Issued Date		Deciphered Date		2013/10/28	
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Document Number		LA-E671P		Rev 1.0	
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P25-Smart AMP / Speaker

LA-E671P

Universal Audio Jack

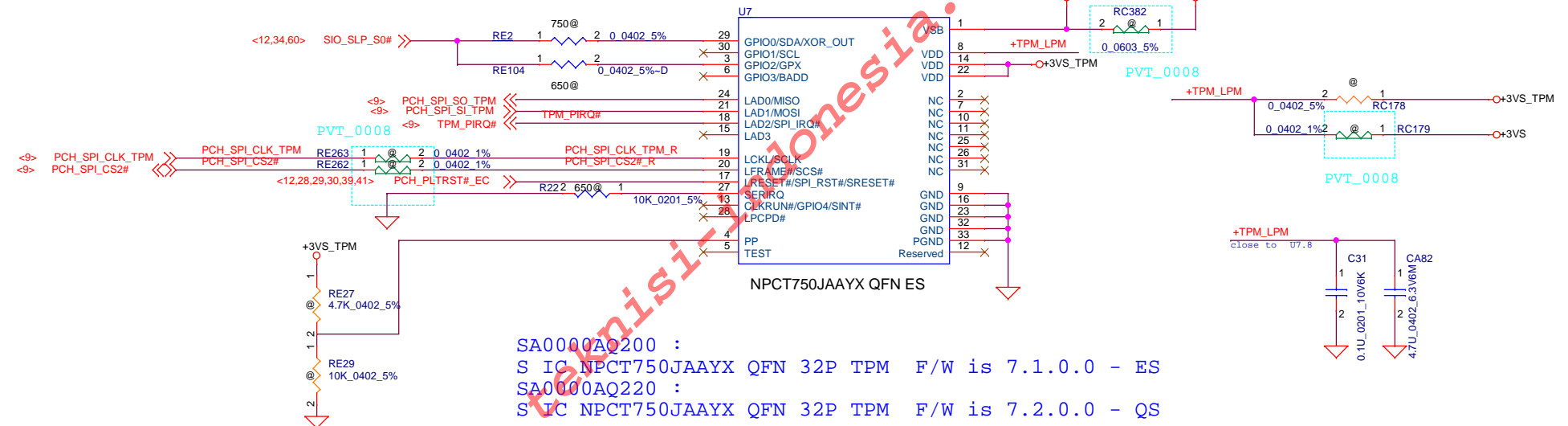
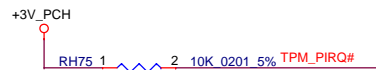
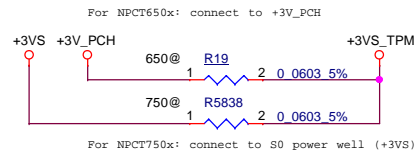


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								Document Number			
								LA-E671P			
								Rev			
								1.0			
								Date: Tuesday, October 17, 2017			
								Sheet 26 of 61			

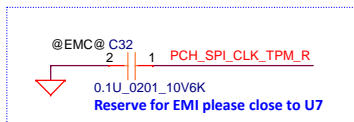
NOTE:
Follow the SPI topology layout guidelines
in the relevant Intel Platform Design Guide

TPM

NOTE:
Place 0.1 uF capacitors as close as
possible to the device power pins



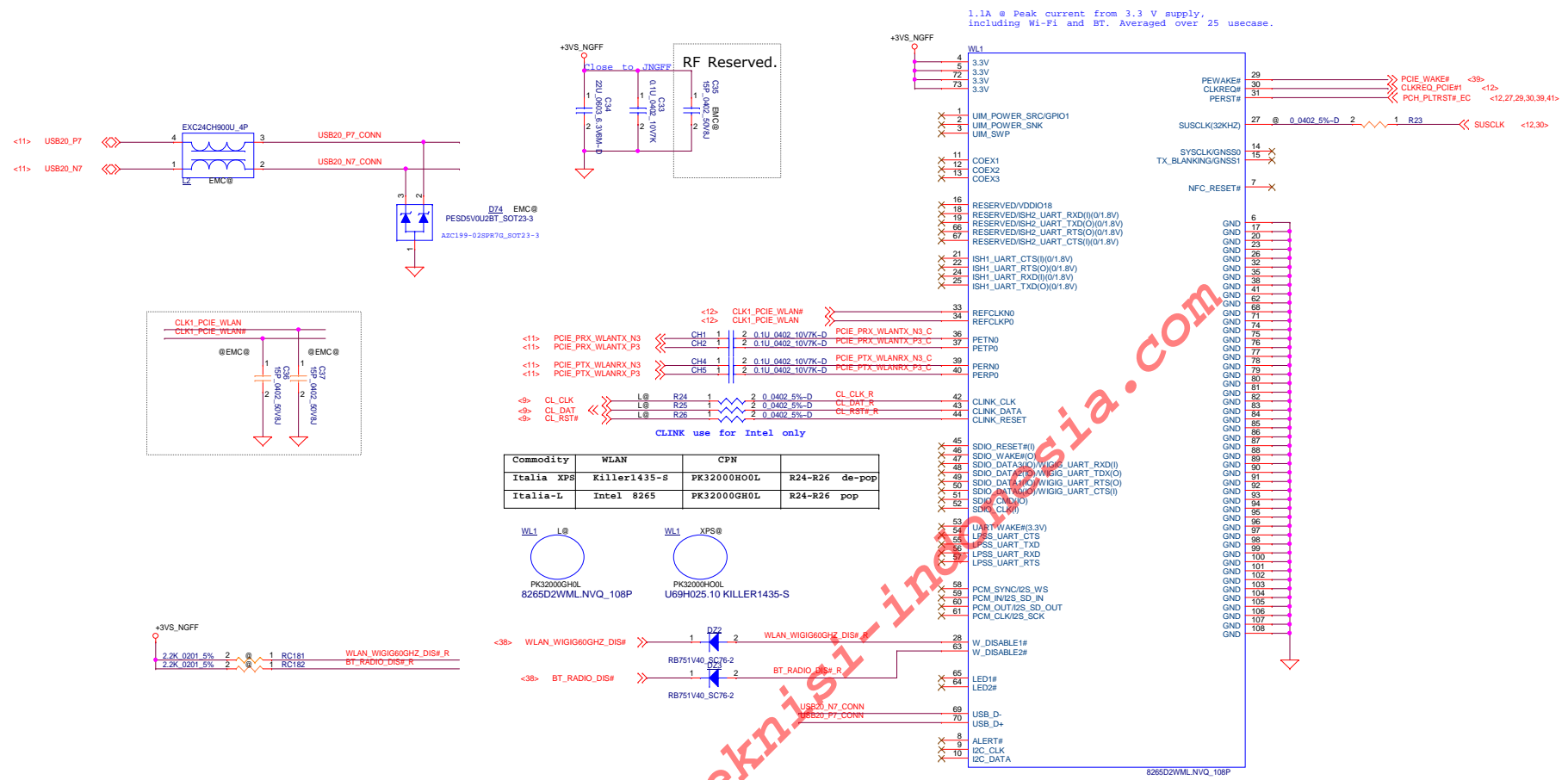
SA0000AQ200 :
S IC NPCT750JAAAX QFN 32P TPM F/W is 7.1.0.0 - ES
SA0000AQ220 :
S IC NPCT750JAAAX QFN 32P TPM F/W is 7.2.0.0 - QS



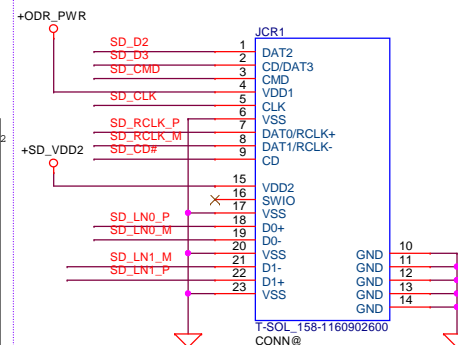
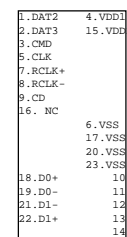
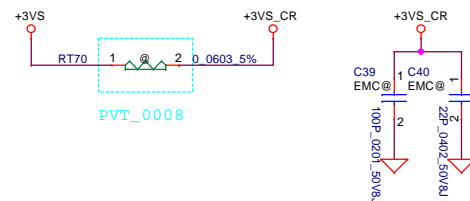
- Pin14&Pin22 (+3VS_TPM):
For NPCT650x: connect to same power well with host SPI interface (it should be +3V_PCH)
For NPCT750x: connect to S0 power well (+3VS)
- Pin27:
For NPCT650x: pop R22
For NPCT750x: de-pop R22
- SLP_S0# connection:
For NPCT650x: pop RE104, de-pop RE2
For NPCT750x: pop RE2, de-pop RE104
- RC180 can be just deleted for both NPCT650x and NPCT750x
- TPM_PIRQ# is recommended that pull-up to same GPIO power well at host side

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				P27-TPM	
				Size	
				Document Number	
				LA-E671P	
				Rev	
				1.0	
				Date:	
				Tuesday, October 17, 2017	
				Sheet	
				27 of 61	

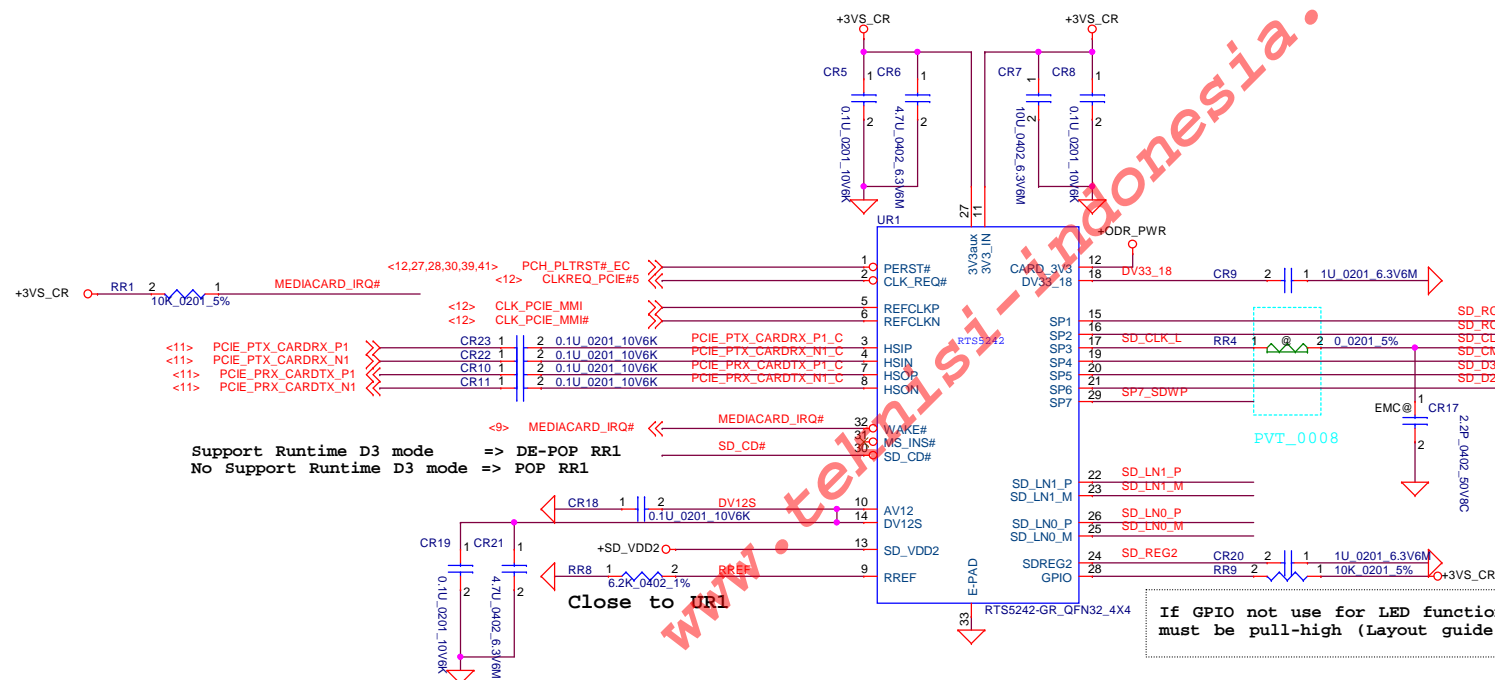
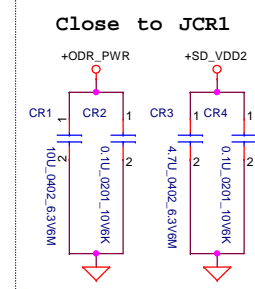
M.2 Slot-A Key-A (WLAN)



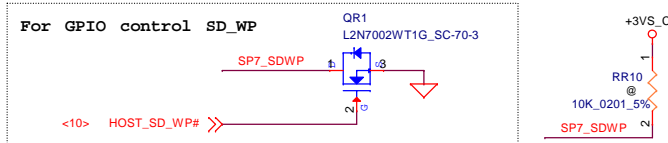
Card Reader



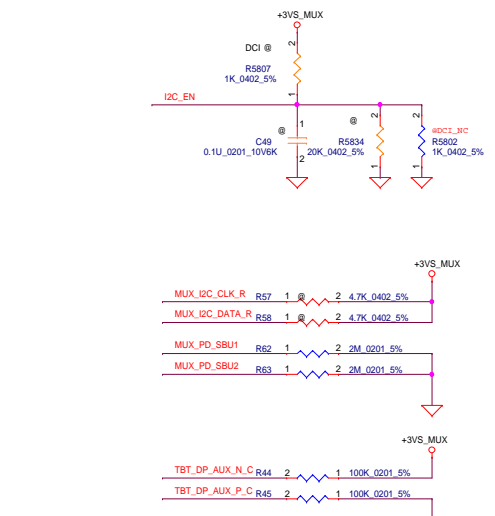
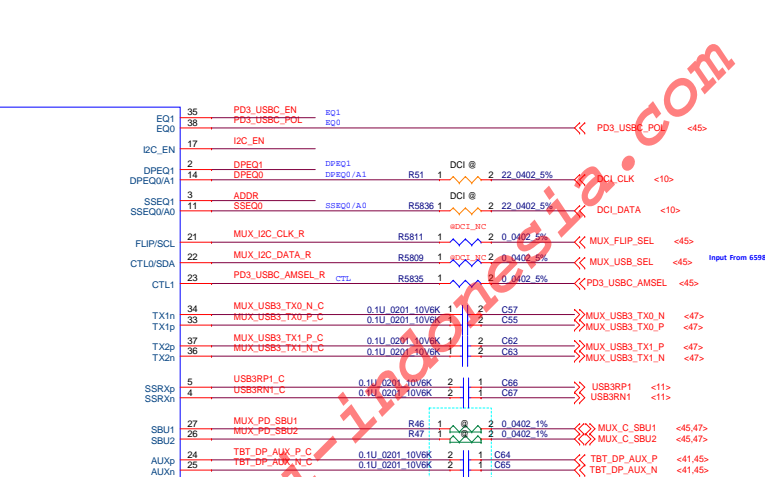
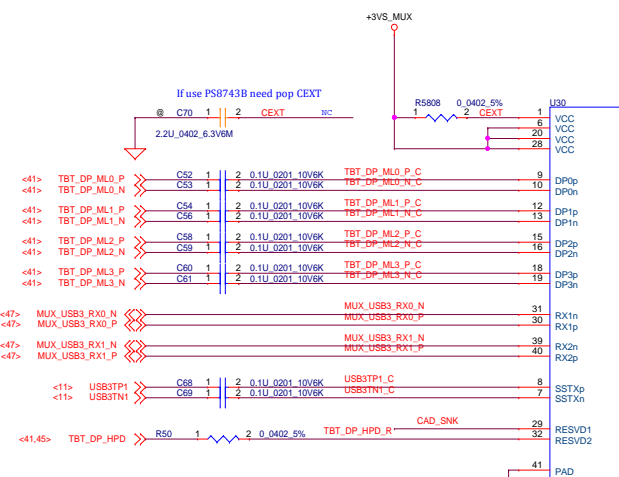
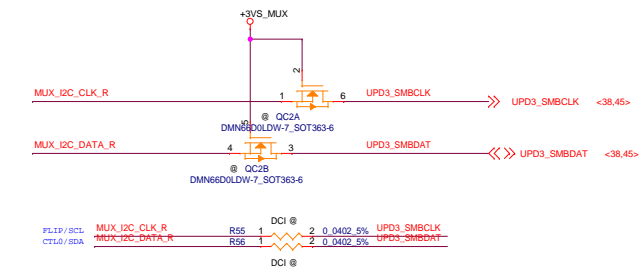
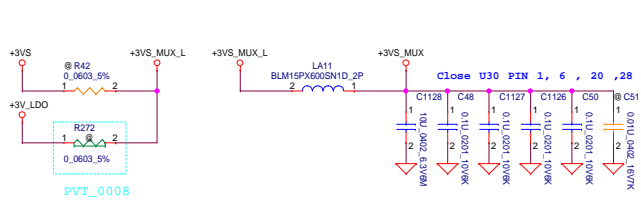
```
Tom0114:wait CIS symbol
TAISOL 158-1160902600 Use LTCX007ZY00
VDD1=ODR_PWR=3.3V
VDD2=SD_VDD2=1.8V
changed footprint & CPN
```



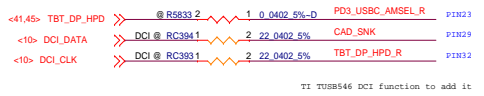
- 1) Placing the RTS5242 chip and flash card socket locate to suit trace routing for SI / EMI / ESD.
- 2) Keep bulk and de-coupling capacitors as close as possible to the RTS5242 chip and flash card socket.
 - Bulk capacitor for Card_3V3 place closed to flash card socket.
 - Bulk capacitor for 3V3_IN / 3V3aux / DV12S place closed to RTS5242 chip.
- 3) Keep damping resistor (ex, for SD CLK / MS CLK) as close as possible to the RTS5242 chip.
- 4) Keep these capacitors for SD card / MS card signals as close as possible to flash card socket.



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				<div> <div> <div>Size</div> <div>Document Number</div> </div> </div>	
				<div> <div> <div>LA-E671P</div> <div> <div>Date: Tuesday, October 17, 2017</div> <div>Sheet 29 of 61</div> </div> </div> </div>	



TUSB546_QFN40_4X6 PVT_0003 PVT_0008
SA00009R720 New CPN for DCI TUSB546A



PIN	DCI	NON-DCI
23 CTL0/HPDIN	DP ENABLE in GPIO mode HPD in I2C mode	DP ENABLE in GPIO mode Unused in I2C mode
29 CAD_SBU/DCI_DAT	AUX Snoop EN in GPIO mode DCI_DAT in I2C mode	AUX Snoop EN in GPIO mode EN in I2C mode
32 DCI_CLK	HPD in GPIO mode DCI_CLK in I2C mode	HPD

- Bring up summary
1. DCI Tools : Frequency HostConfig.xml file change to Clk133MHz = 2
 2. EC updated TUSB546 reg[0x0A] bit 4 for EQ controlled by I2C.
 3. Pop DCI @ HW parts and Depop @ DCI_NC / PCH RC29 up to 4.7K ohm
 4. For DCI BIOS

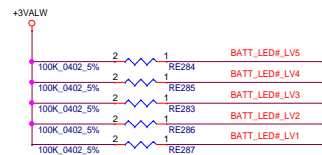
LEVEL	SETTINGS
0	Option 1: Tie 1k ohm 5% to GND Option 2: Tie directly to GND
R	Tie 20K ohm 5% to GND
F	Float (leave pin open)
1	Option 1: Tie 1k ohm 5% to VCC Option 2: Tie directly to VCC

TUSB546 MUX default H/W setting

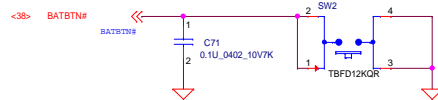
CTL1 EN (Pin 23)	CTL0 AMSEL (Pin 22)	FLUP PCH (Pin 21)	TUSB546 Configuration	VESA DisplayPort Alt Mode (DP1.0 Configuration)
L	L	L	Power Down	
L	L	H	Power Down	
L	H	L	One Port USB 3.1 - No Flip	
L	H	H	One Port USB 3.1 - With Flip	
H	L	L	4 Lane DP - No Flip	C and E
H	L	H	4 Lane DP - With Flip	C and E
H	H	L	One Port USB 3.1 + 2 Lane DP - No Flip	D and F
H	H	H	One Port USB 3.1 + 2 Lane DP - With Flip	D and F

Device Configuration in GPIO Mode

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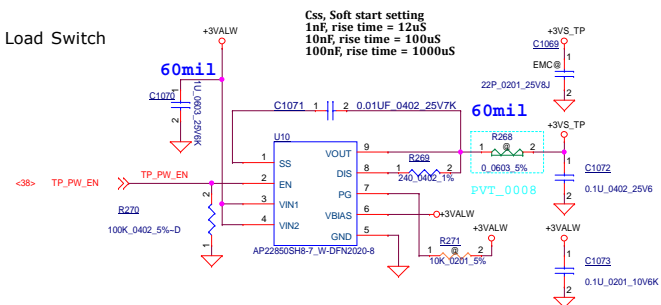
Batry Gagne Buton



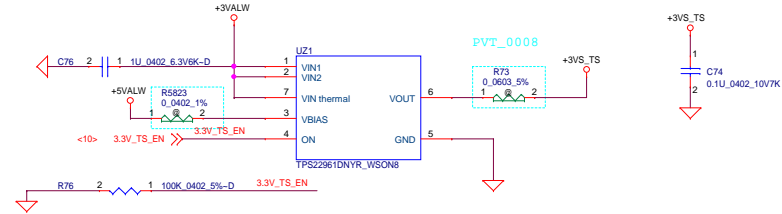
Compal Electronics, Inc.

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		Deciphered Date		<div style="text-align: right;"> LA-E671P </div>	
		2016/12/13		<div style="text-align: right;"> Rev 1.0 </div>	
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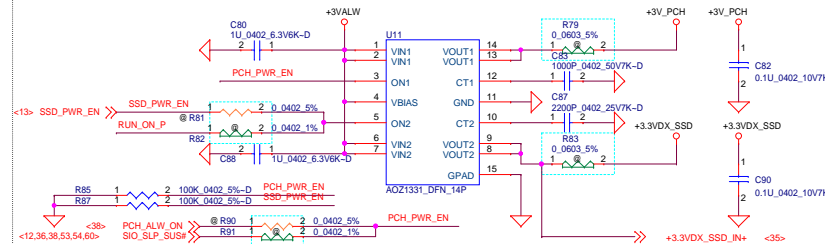
Touch Pad Load Switch



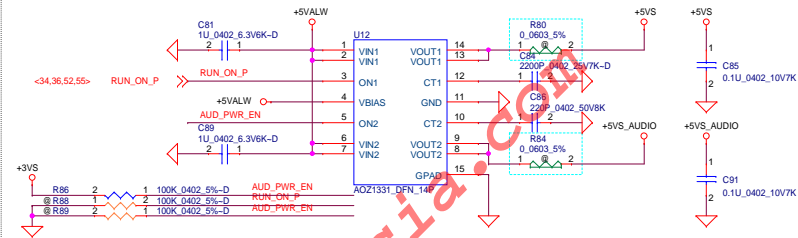
Touch Screen Load Switch



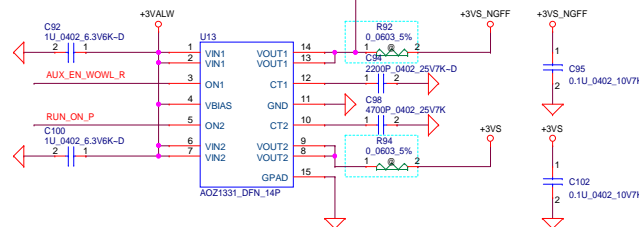
Deeper Sleep, SSD Load Switch



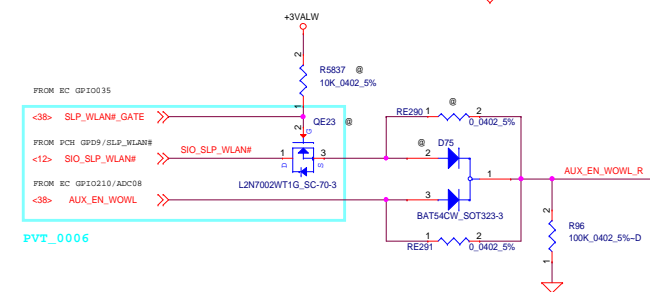
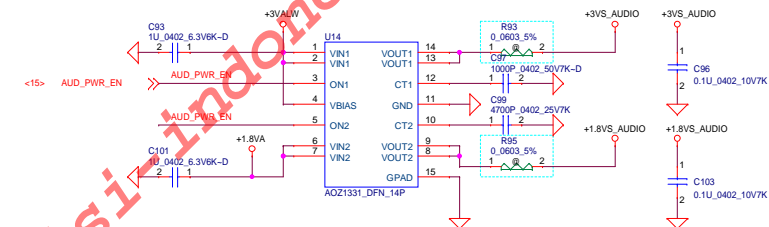
5V_Run, 5V_Audio Load Switch



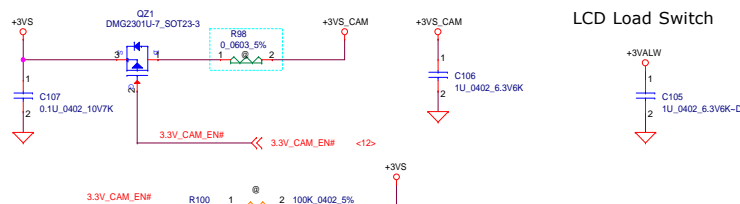
WiFi, 3V_RUN Load Switch



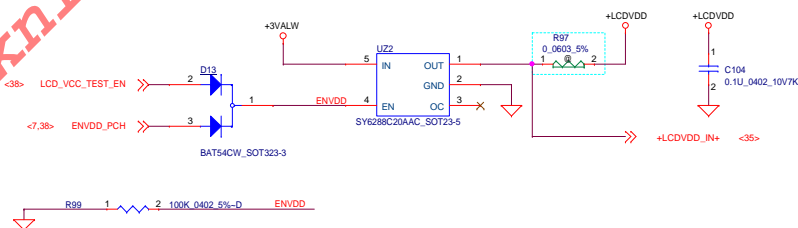
3V_Audio, 1.8V_Audio Load Switch



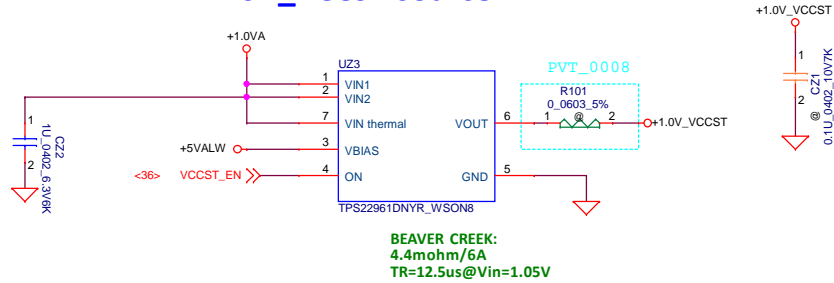
Camera



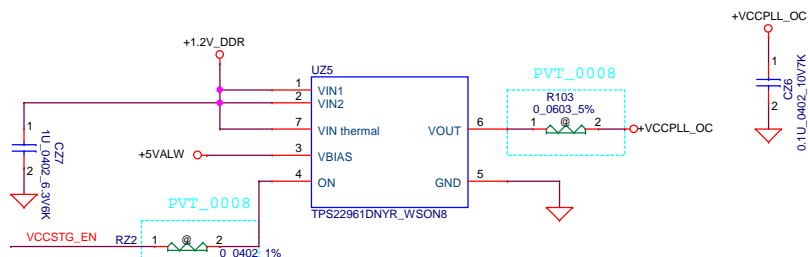
LCD Load Switch



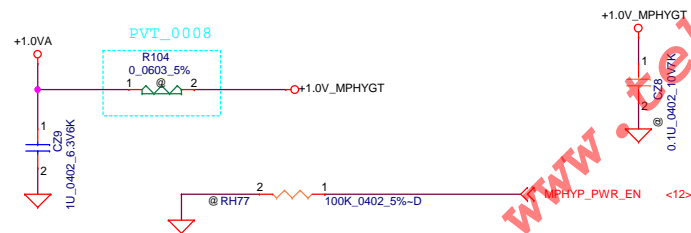
+1.0V_VCCST source



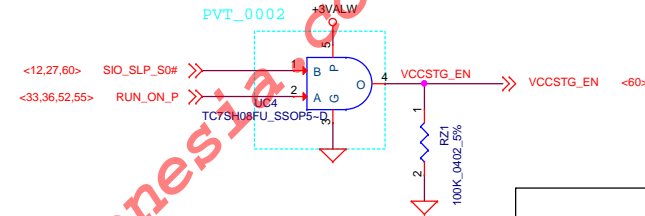
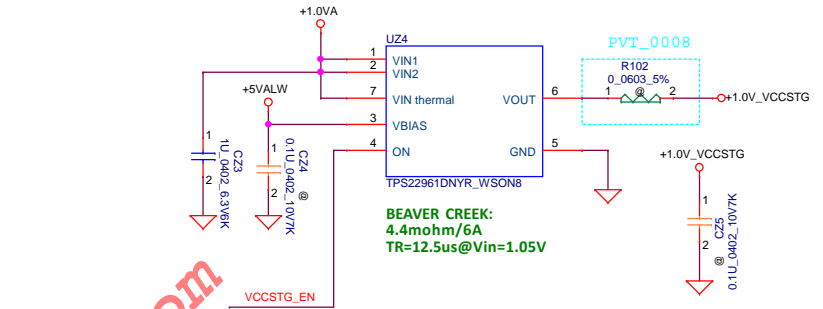
+VCCPLL_OC source



+1.0V_MPHYGT source



+1.0V_VCCSTG source

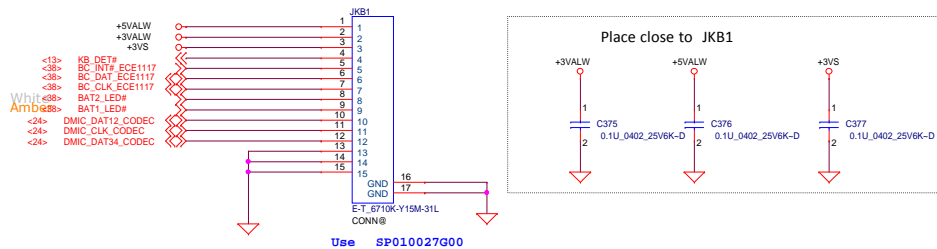


	S0	S0Ix	S3
SIO_SLP_S0#	high	low	low
RUN_ON_EC	high	high	low

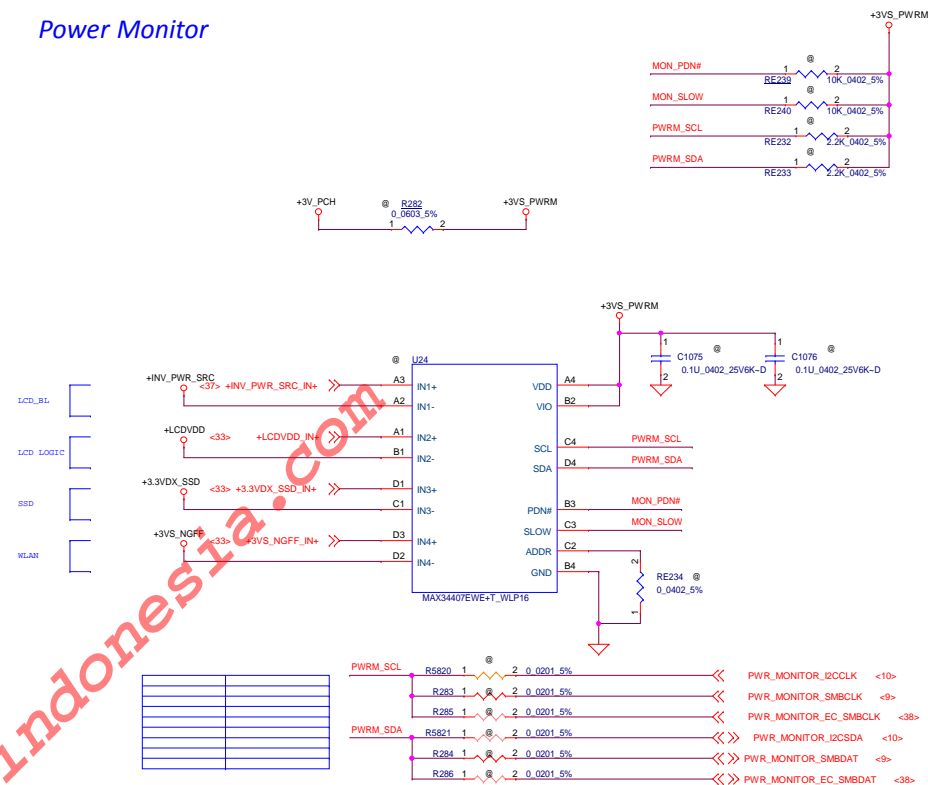
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Title P34-DC/DC Interface 2			
Size	Document Number	Rev	
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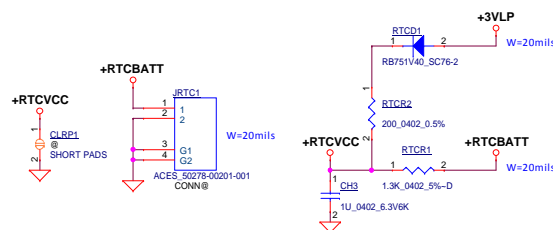
Keyboard Controller board + DMIC



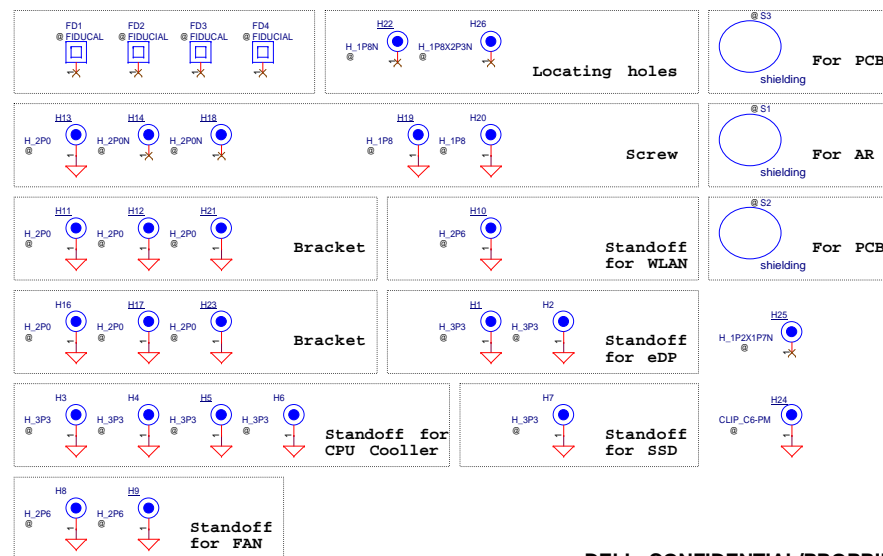
Power Monitor



RTC Battery With Charge Function



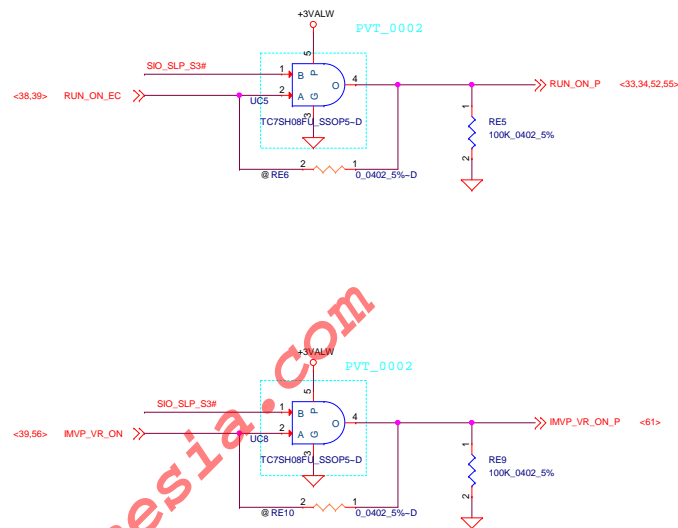
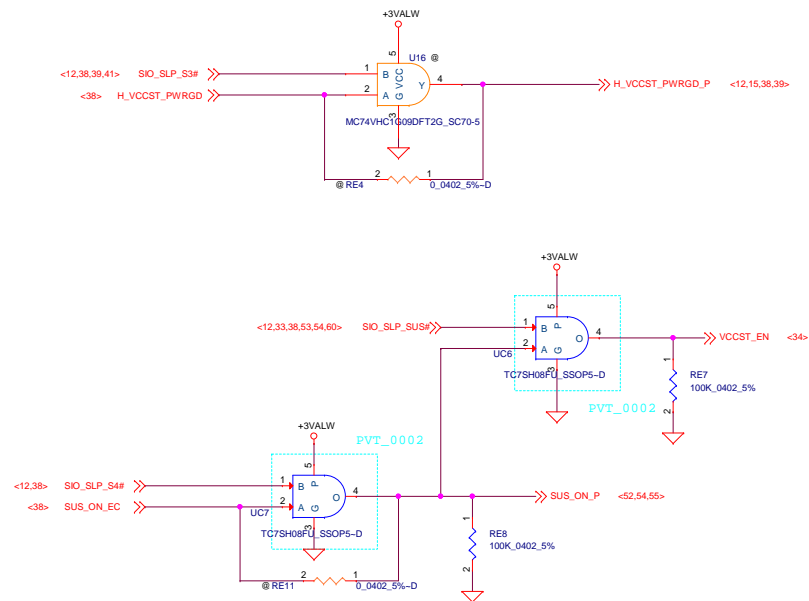
SCREW Hole



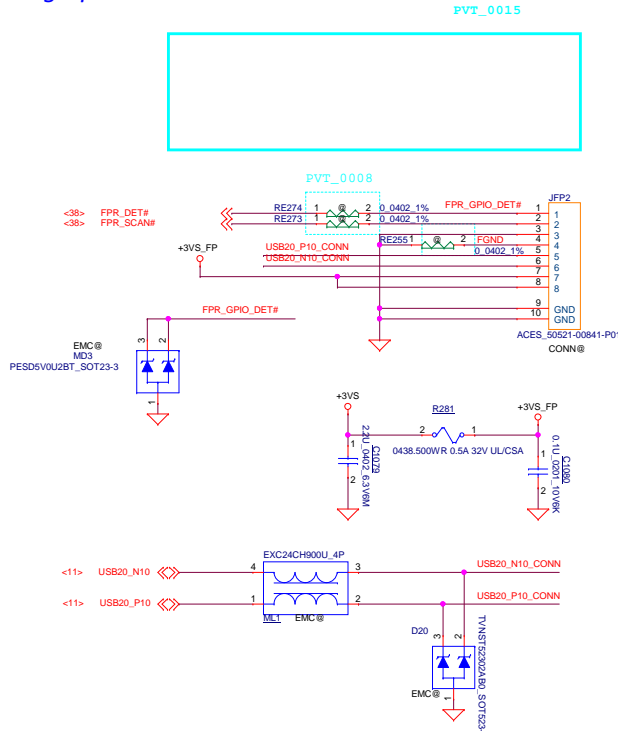
DELL CONFIDENTIAL/PROPRIETARY

Compal Secret Data

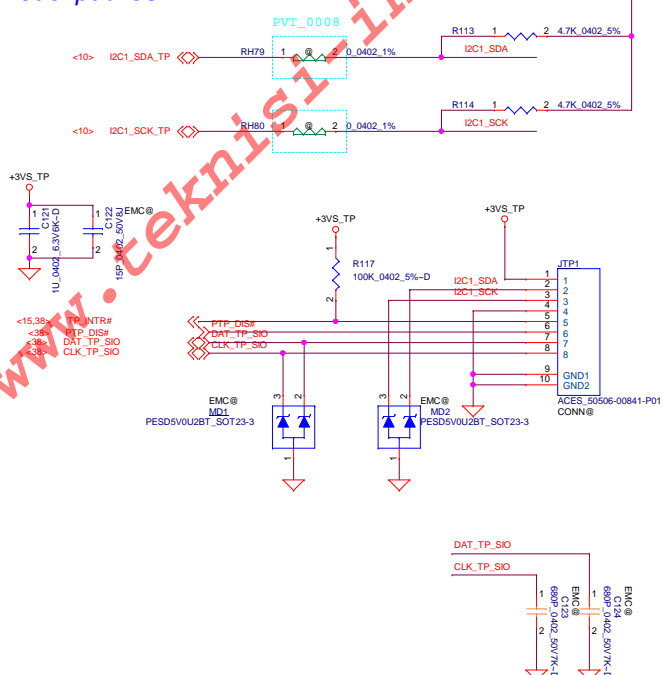
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Issued Date	2015/12/16	Deciphered Date	2016/12/13	Size	Document Number	Rev 1.0
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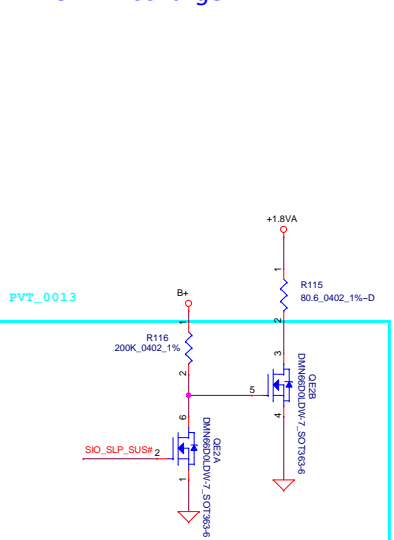
Fingerprint CONN



Touchpad CONN

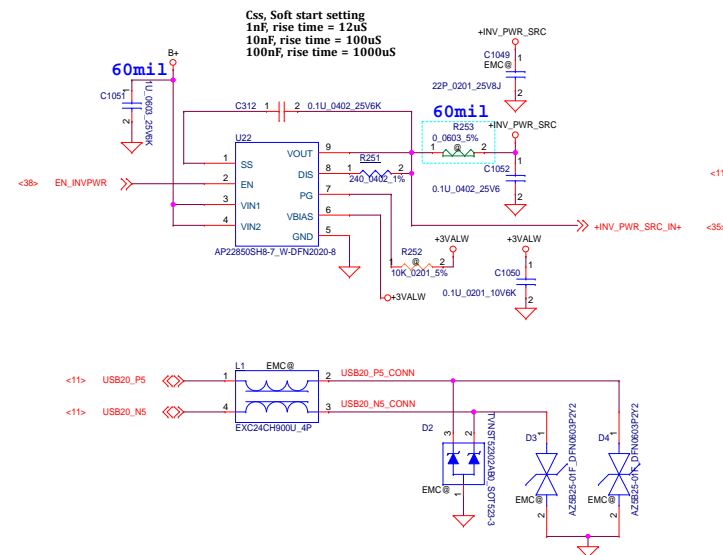


+1.8VA Discharge

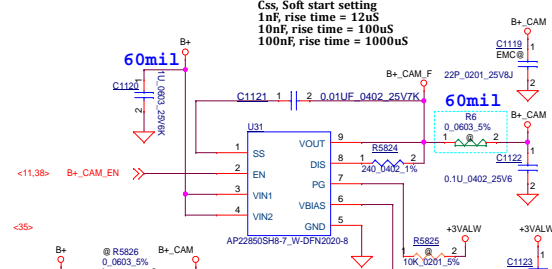


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Css, Soft start setting
1nF, rise time = 12uS
10nF, rise time = 100uS
100nF, rise time = 1000uS



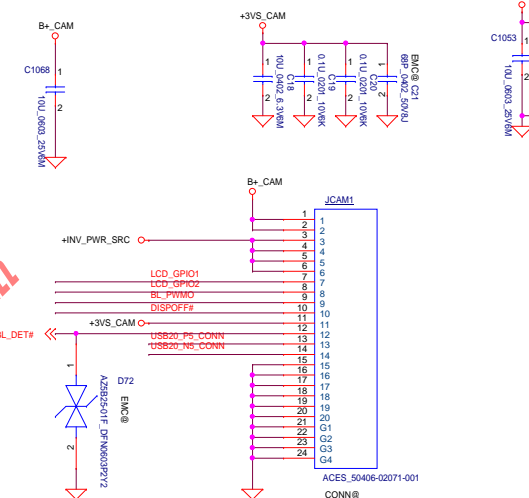
Css, Soft start setting
1nF, rise time = 12uS
10nF, rise time = 100uS
100nF, rise time = 1000uS



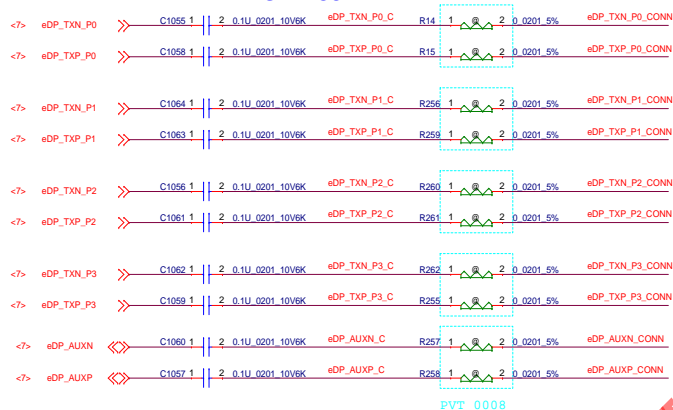
CAM & IR CAM

LCD BL Power

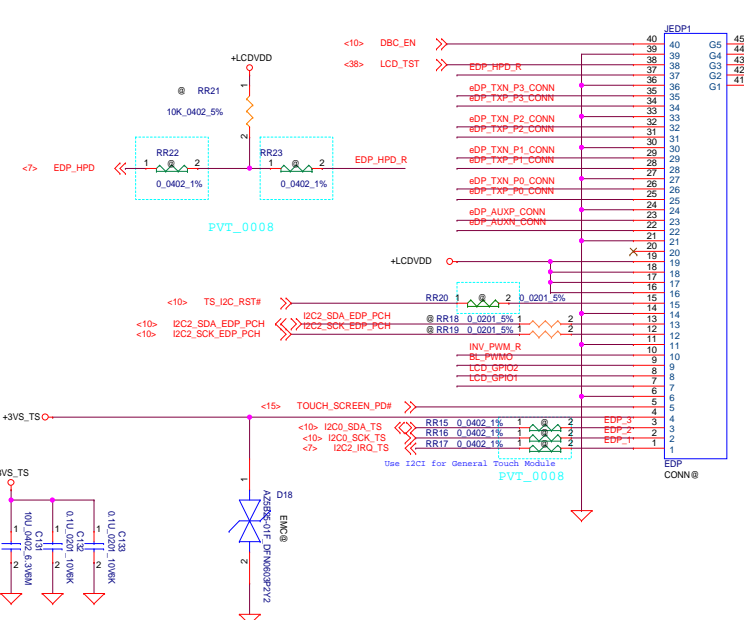
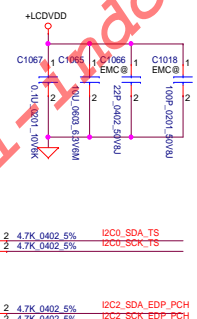
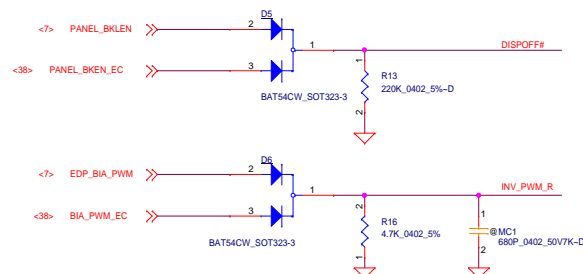
CAM & IR CAM



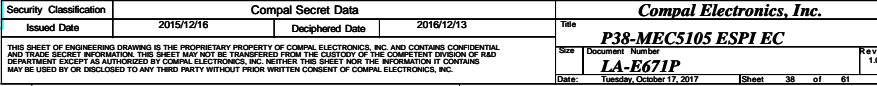
eDP Conn



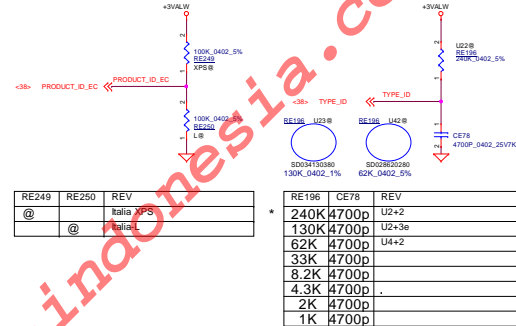
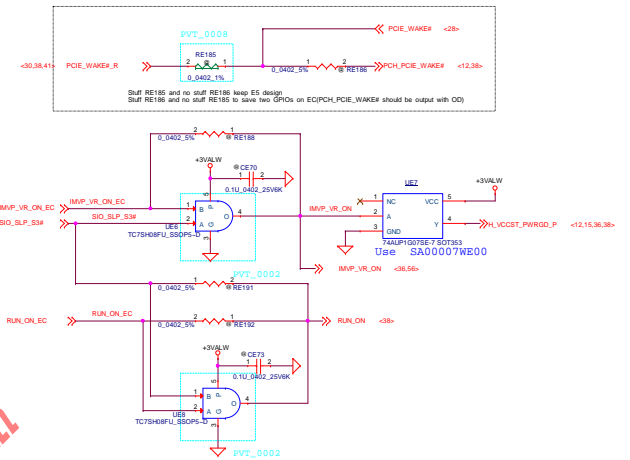
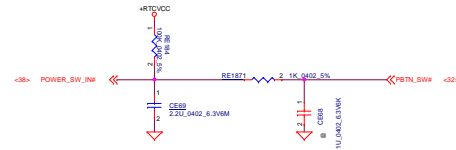
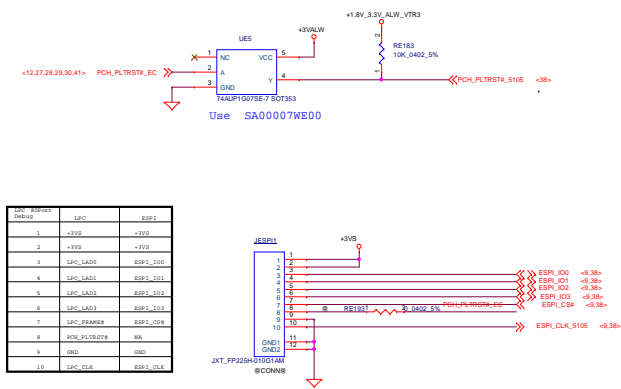
BackLight PWM Control



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2041/09/08		2013/10/28		P37-eDP+TS & CAM+BL CONN	
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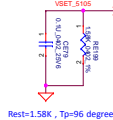
QFN Pinout	QFN	QFN
1	VDD	VDD
2	VDD	VDD
3	VDD	VDD
4	VDD	VDD
5	VDD	VDD
6	VDD	VDD
7	VDD	VDD
8	VDD	VDD
9	VDD	VDD
10	VDD	VDD



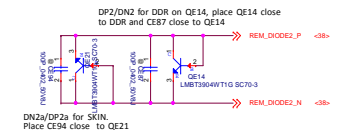
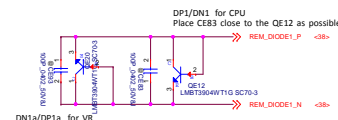
RE194	CE75	REV
240K	4700p	X00
130K	4700p	X01
62K	4700p	X02
33K	4700p	X03
8.2K	4700p	A00
4.3K	4700p	
2K	4700p	
1K	4700p	

BOARD_ID rise t1 nbs meas uedfro m5 %68 %

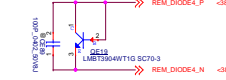
PANEL_ID rise t1 nbs meas uedfro m5 %68 %



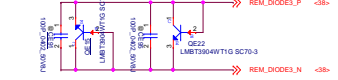
5105 Channel	Locat i on
DP1/DN1	OTP (QE12)
SEN4	DN1a/DP1a Charger (QE20)
SEN1	DP2/DN2 DDR (QE14)
SEN5	DN2a/DP2a SKIN (QE21)
SEN6	DP3/DN3 SKIN (QE22)
SEN2	DN3a/DP3a SSD (QE15)
SEN3	DP4/DN4 WLAN (QE19)
	DN4a/DP4a



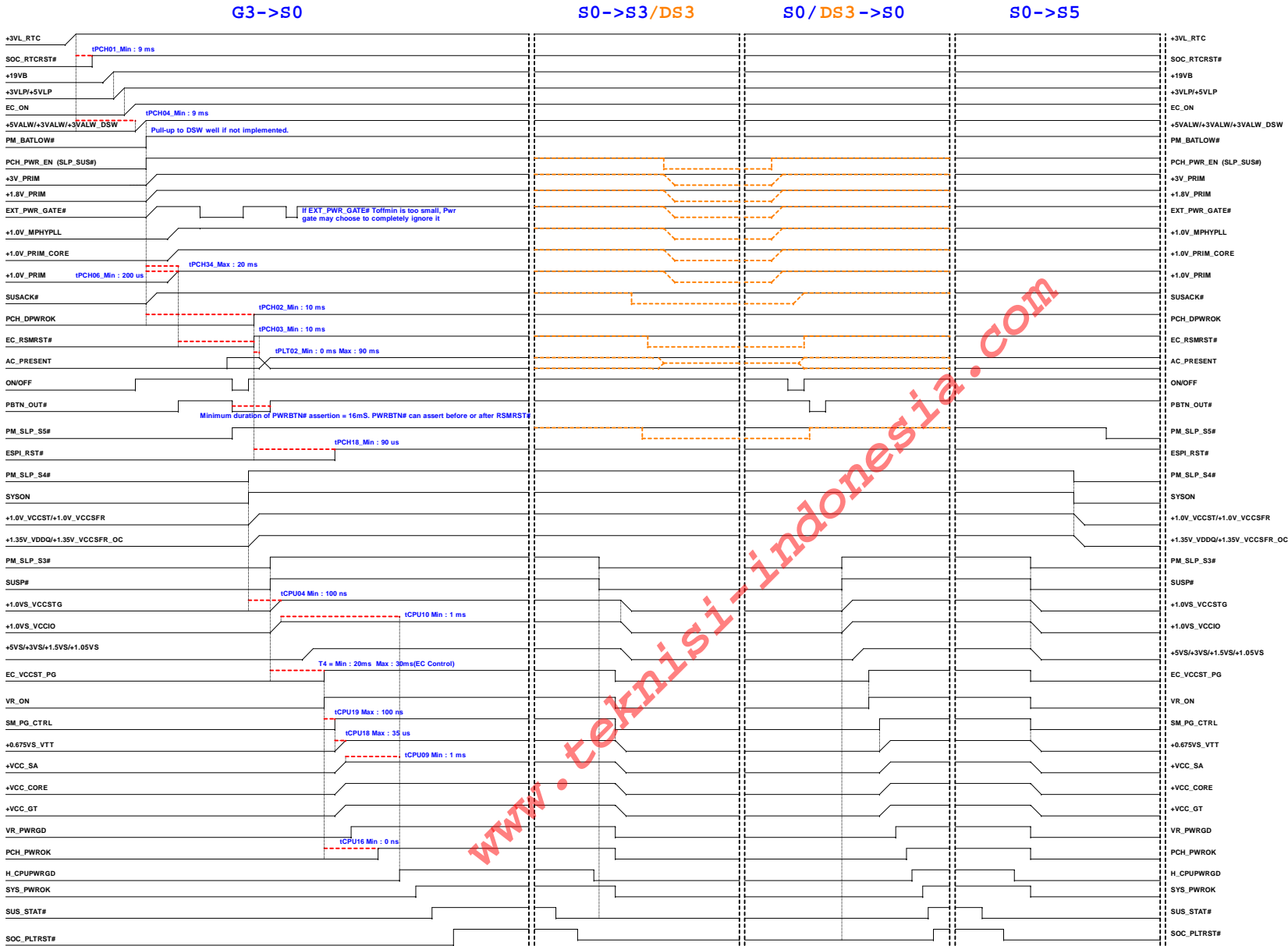
DP4/DN4 for WLAN on QE19, place QE19 close to WLAN & QE19 close to CE89.

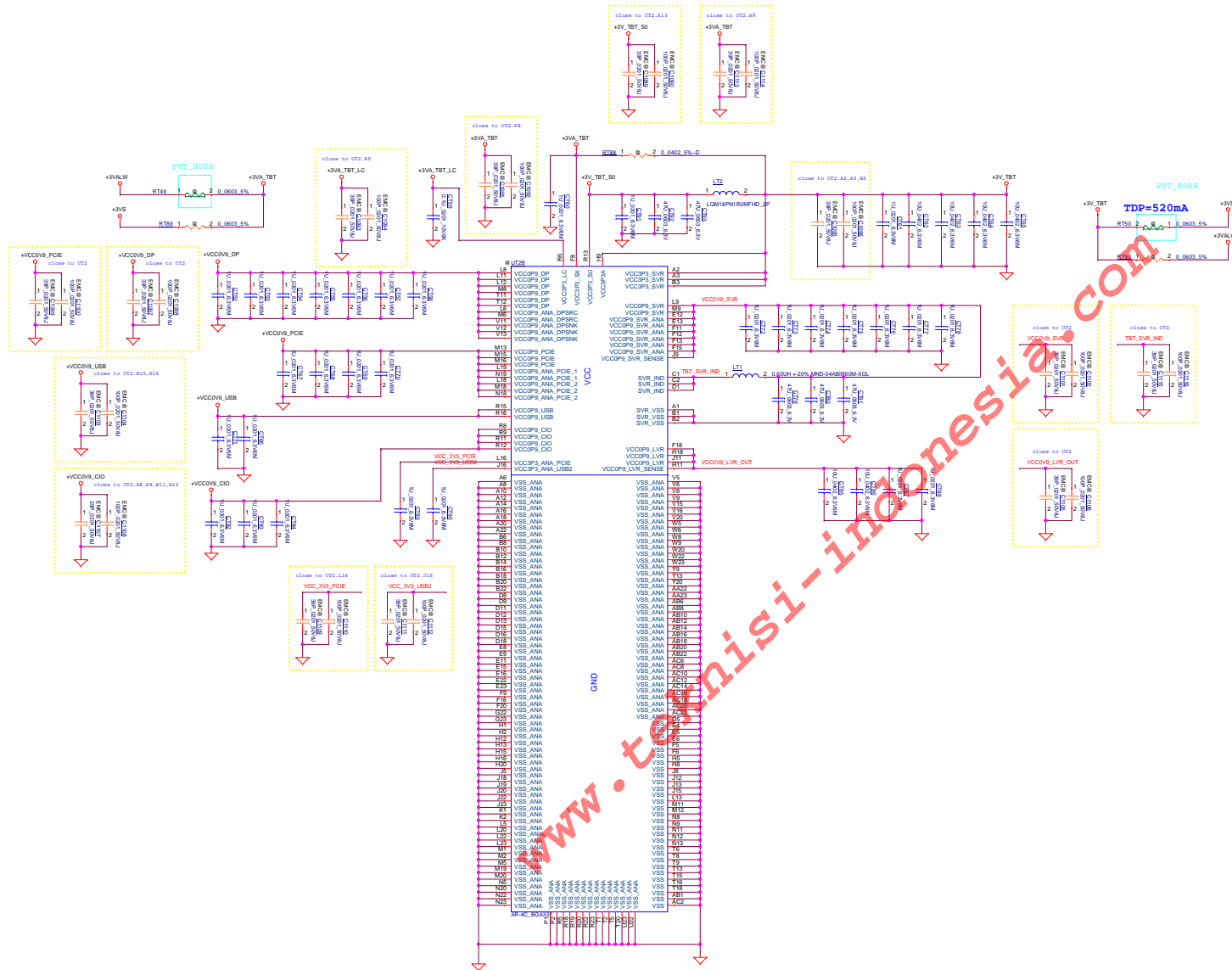


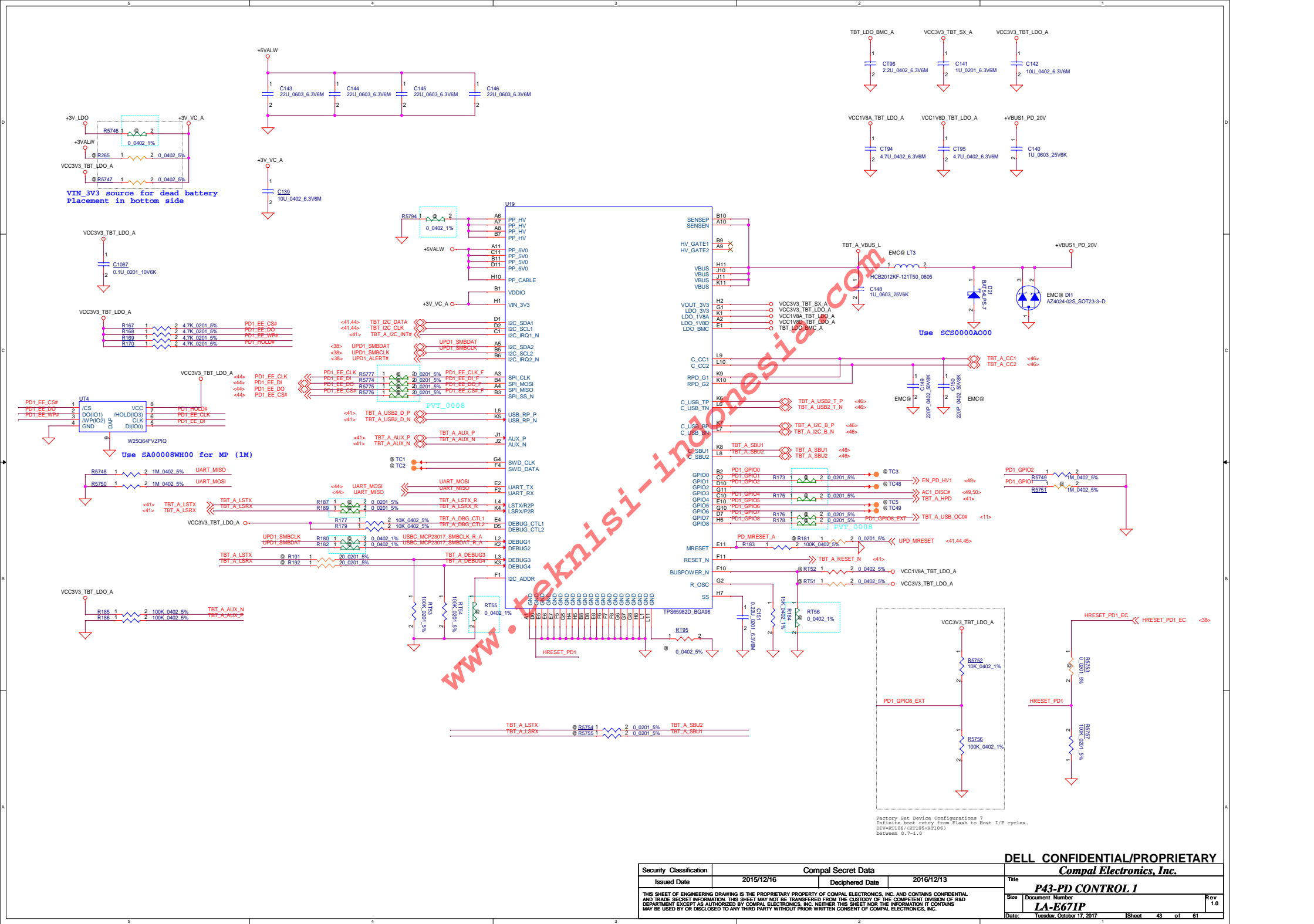
DP3/DN3 for SSD Place CE91 close to the QE15 as possible



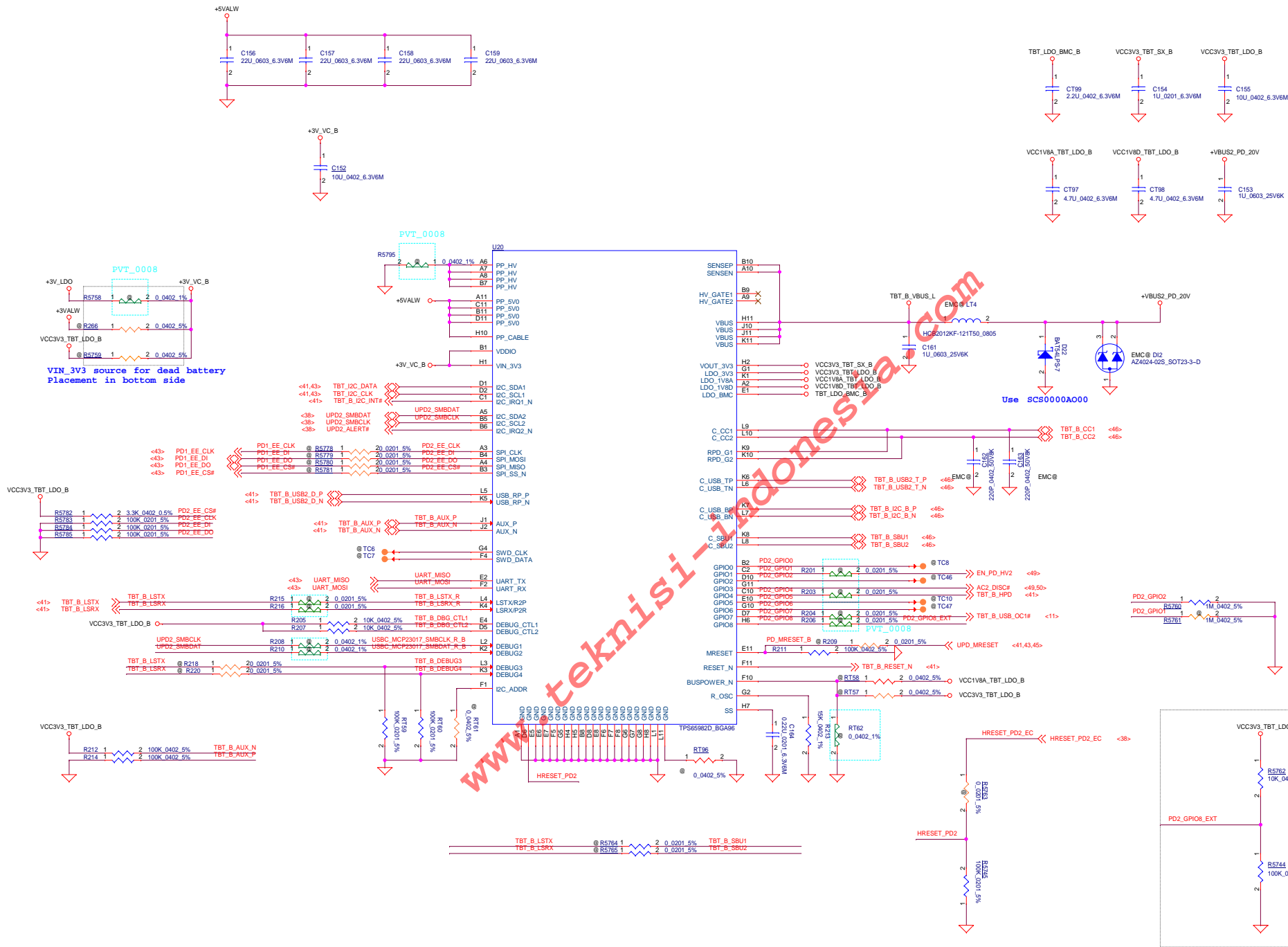
DN3a/DP3a for TSD Place CE95 close to QE22



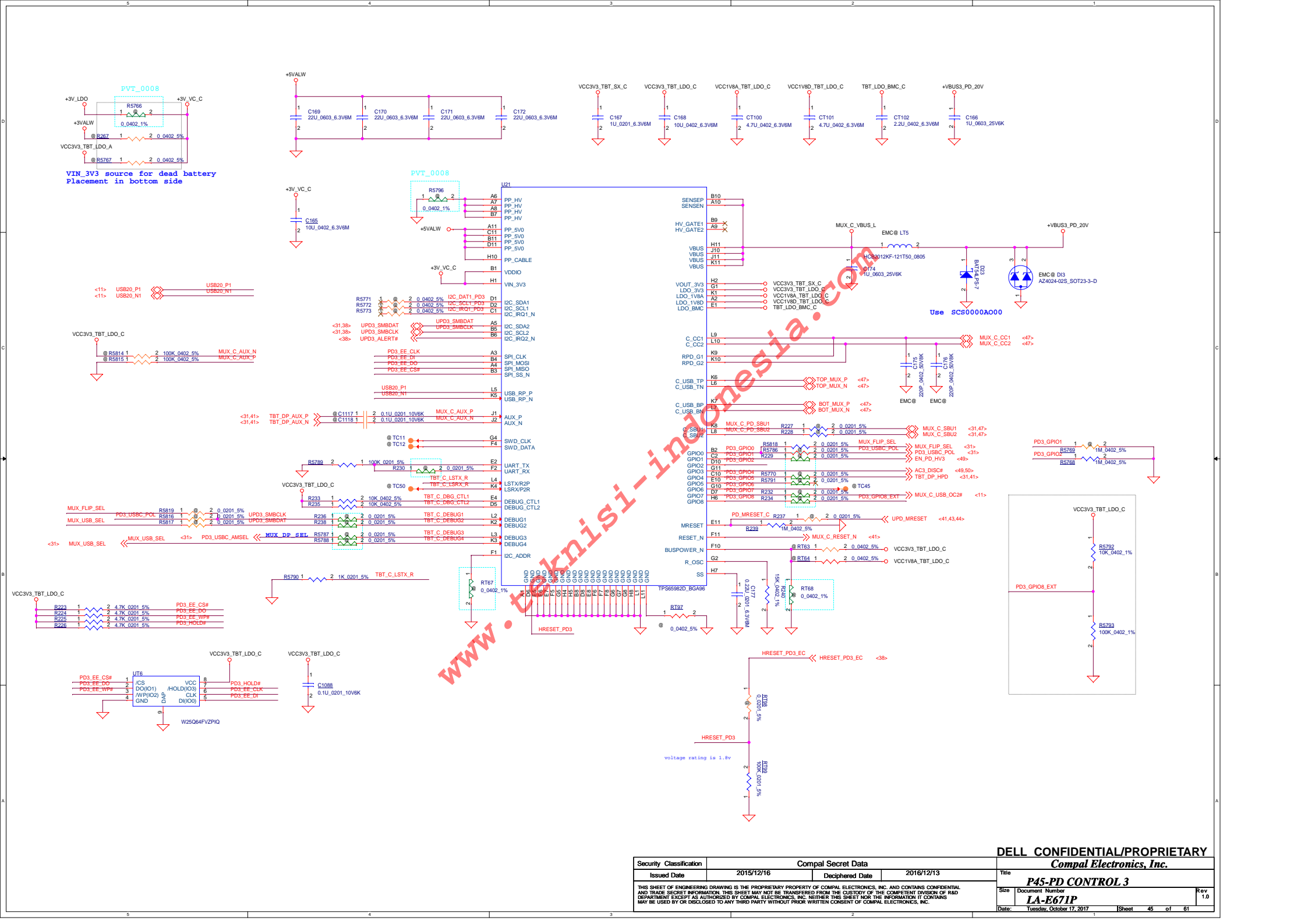


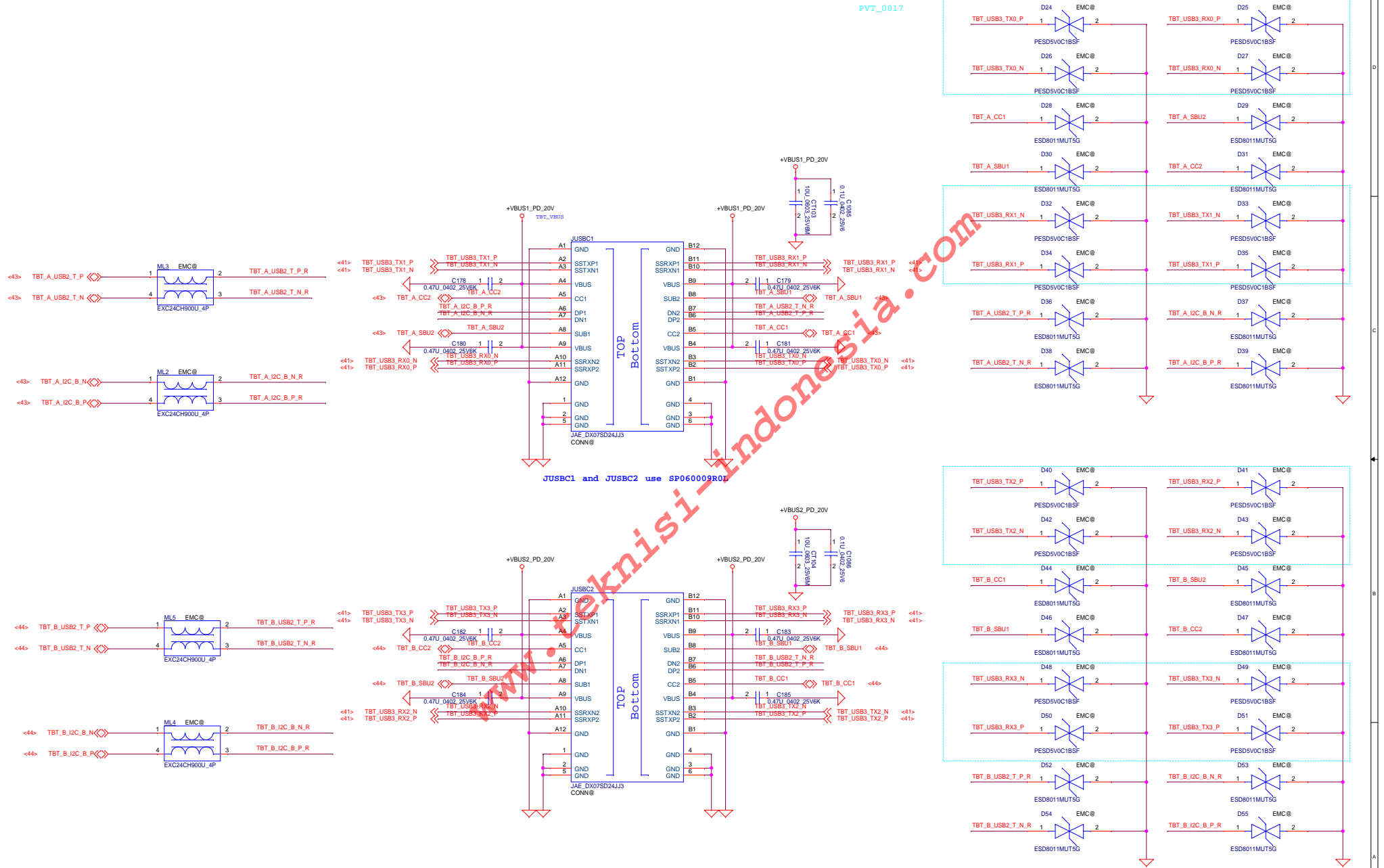


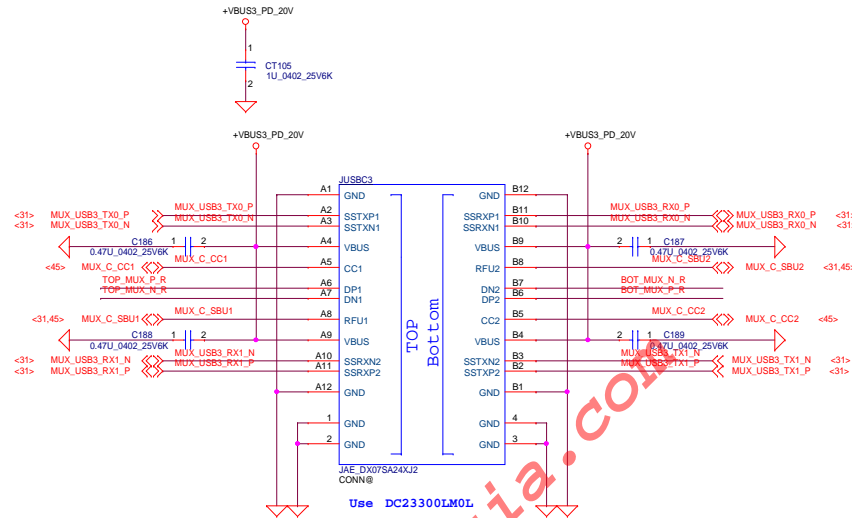
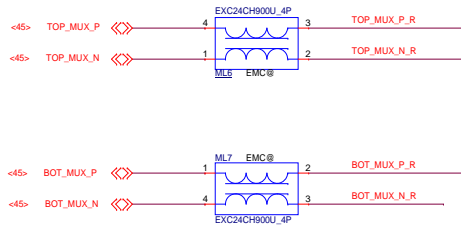
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				Document Number	
				LA-E671P	
				Date	
				Tuesday, October 17, 2017	
				Sheet	
				43 of 61	
				Rev	
				1.0	



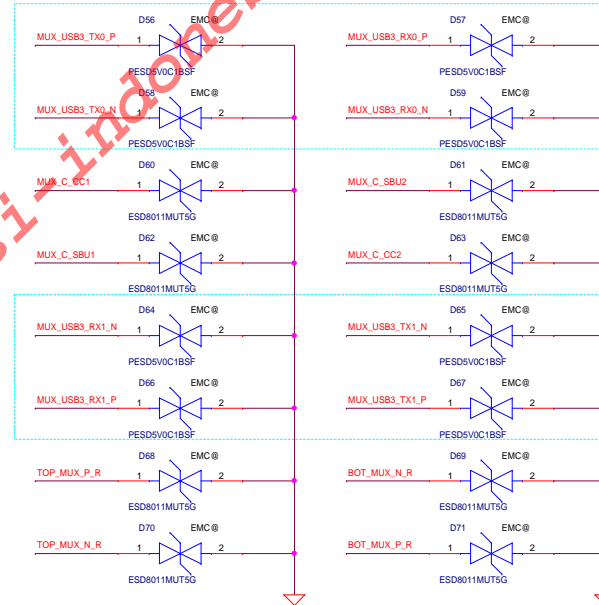
Security Classification		Compal Secret Data		DELL CONFIDENTIAL/PROPRIETARY	
Issued Date		2015/12/16		Deciphered Date	
				2016/12/13	
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				P44-PD CONTROL 2	
Size		Document Number		Rev	
		LA-E671P		1.0	
Date:		Tuesday, October 17, 2017		Sheet 44 of 61	







PVT_0017



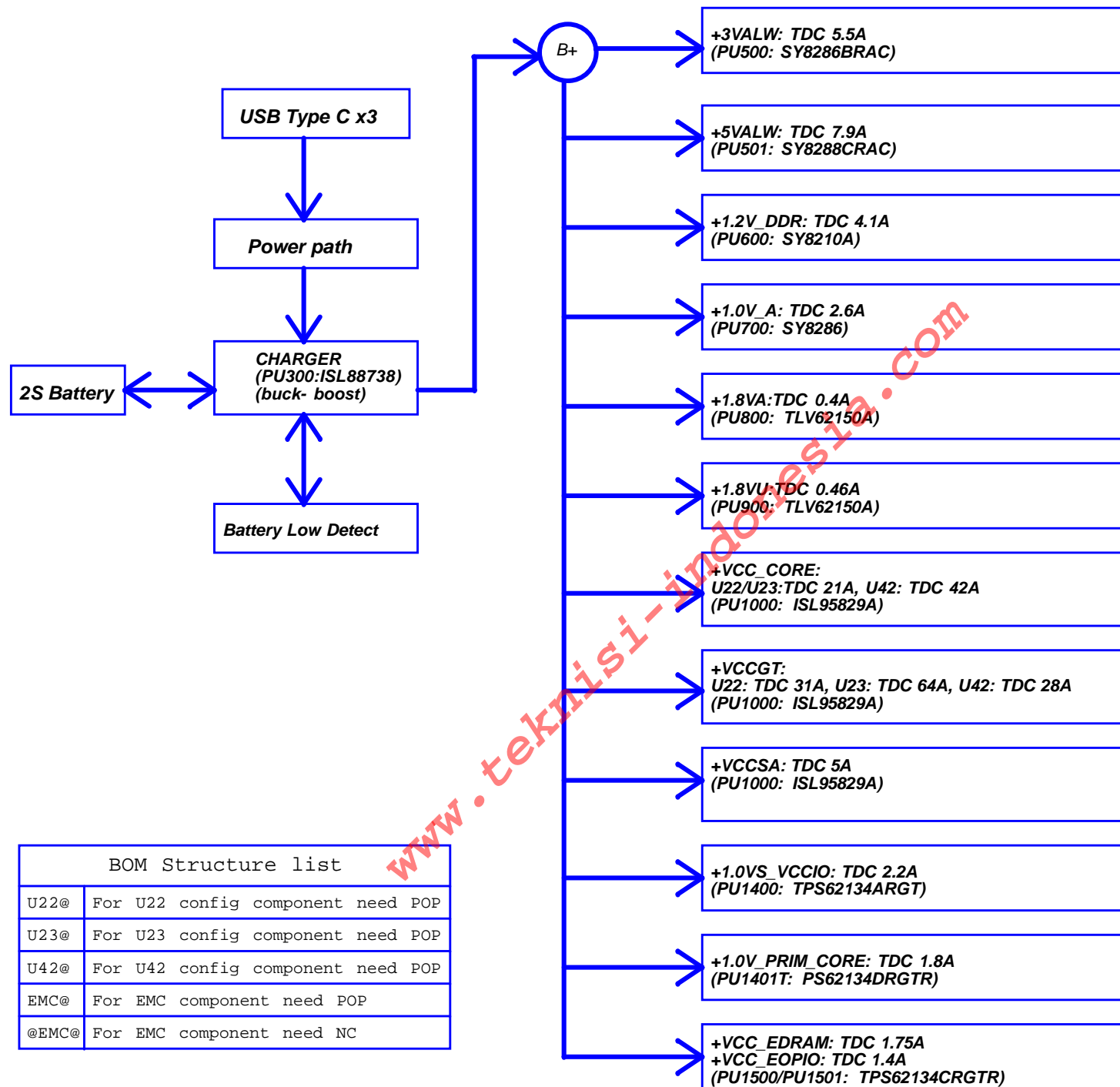
DELL CONFIDENTIAL/PROPRIETARY

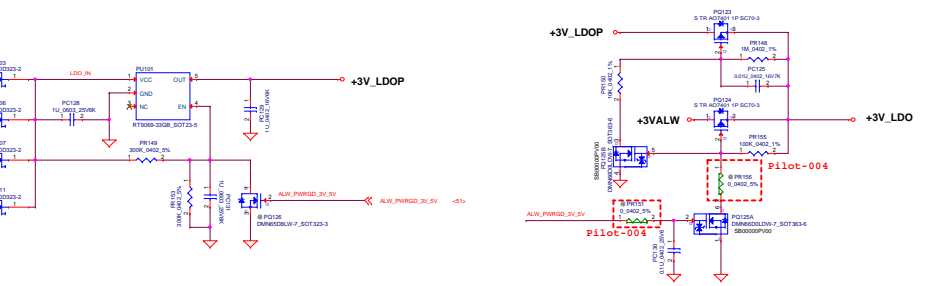
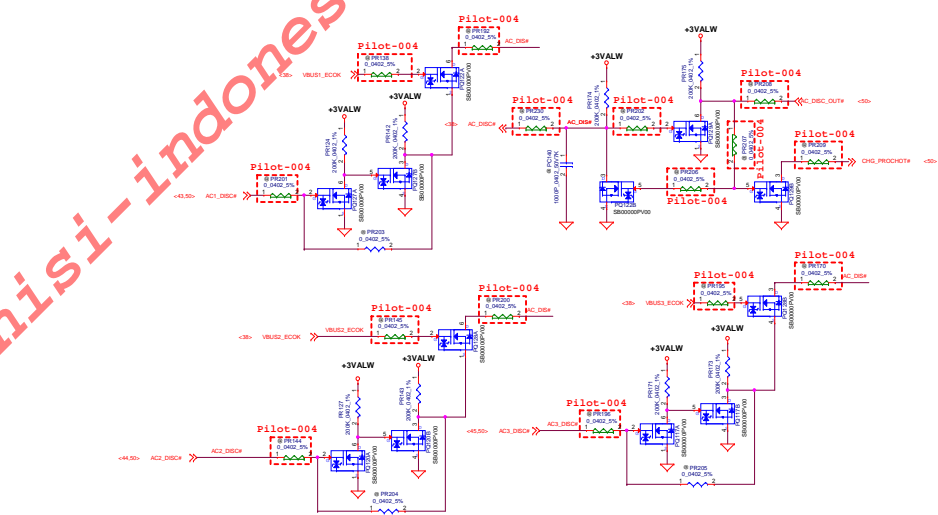
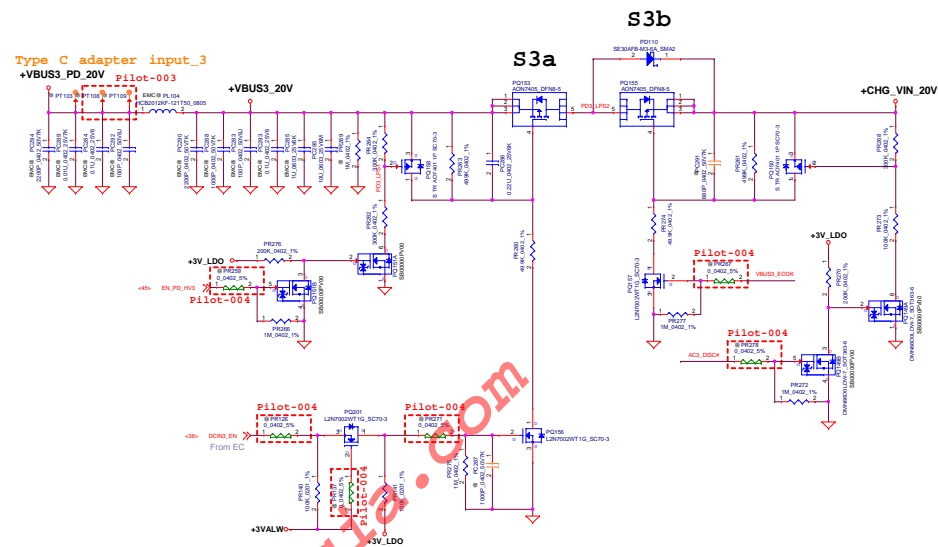
Compal Electronics, Inc.

P47-PD USB TYPE-C 3

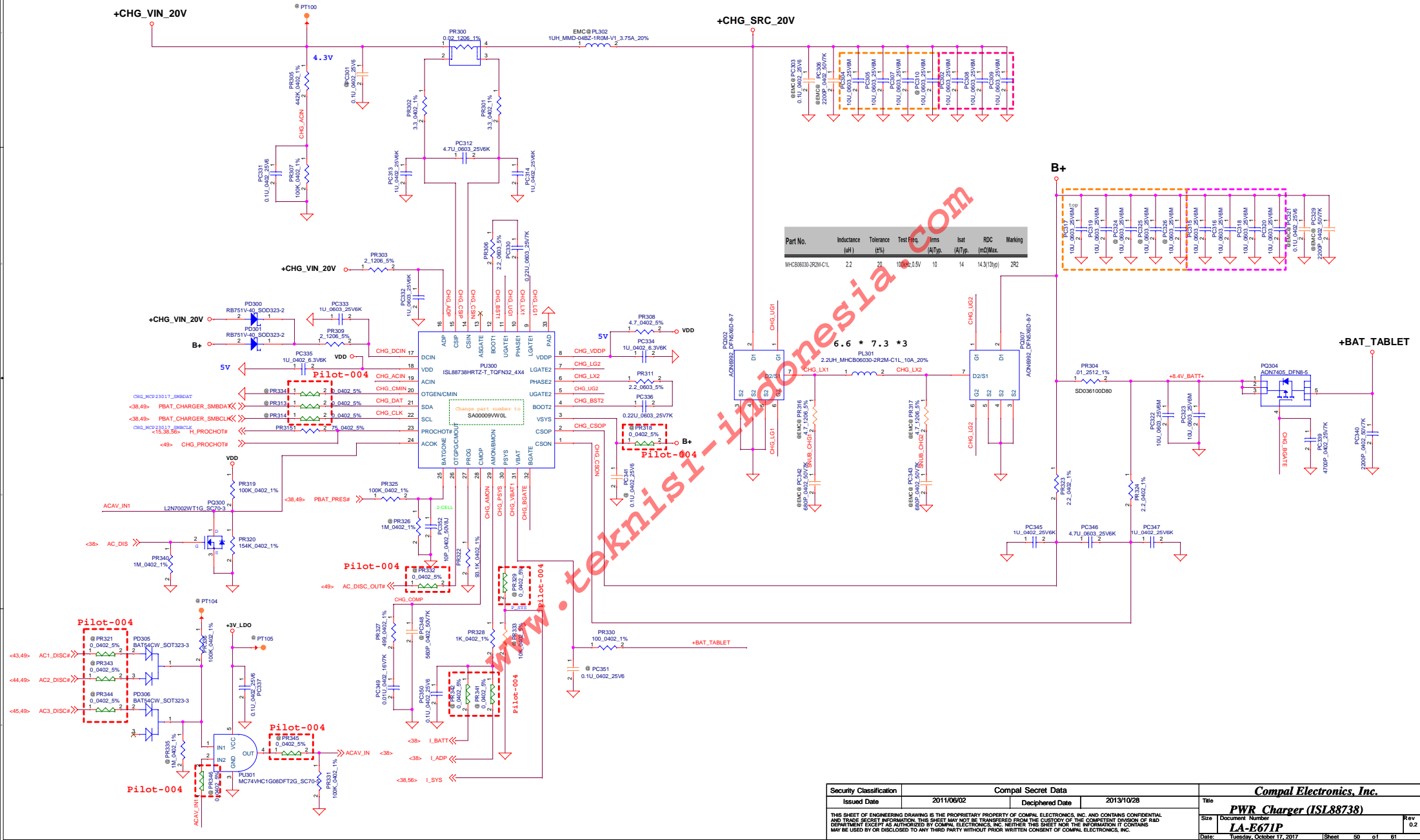
Size Document Number Rev
C LA-E671P 1.0
Date: Tuesday, October 17, 2017 Sheet 47 of 61

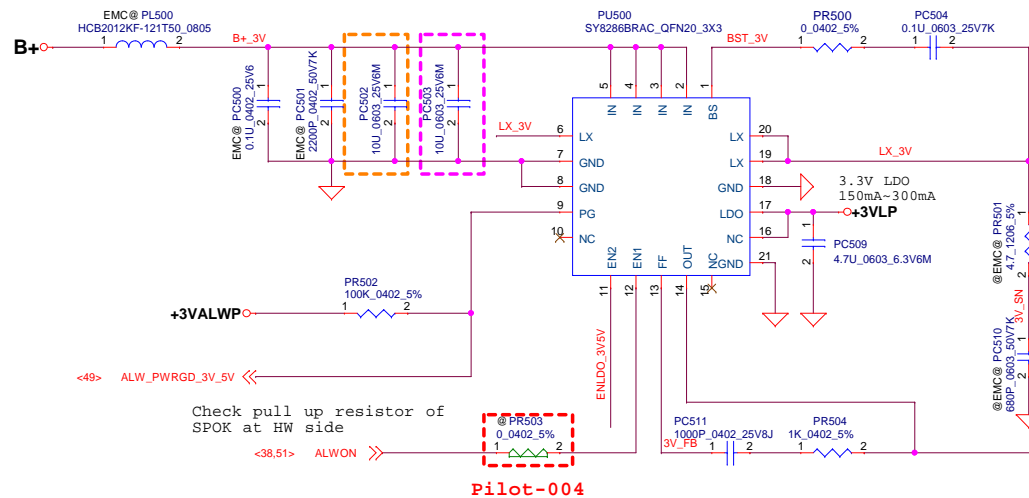
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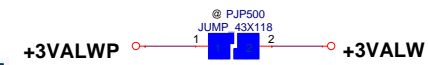


Security Classification		Compal Secret Data		Compal Electronics, Inc. DCIN/Power Path	
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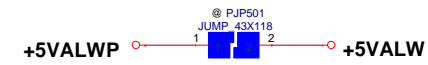
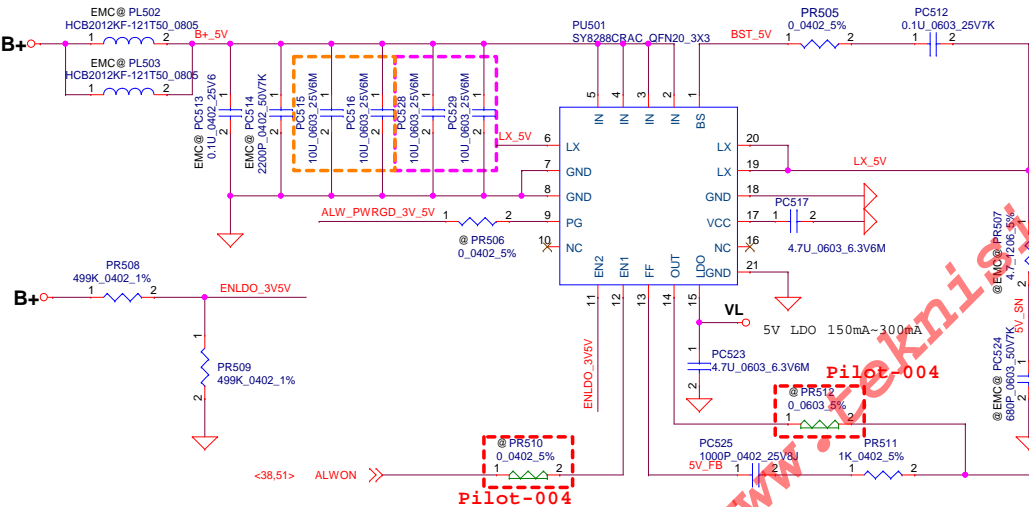
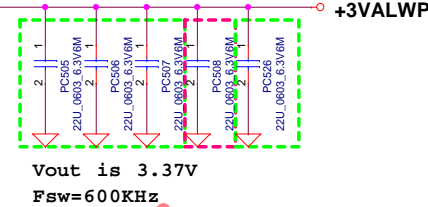


P/N	L*W(mm*mm)	H(mm)	Lx(μH)	RDC(mΩ)	Ids(A)	Isat(A)
MMD-05CZ-1R5M-V1L	5.49*5.18	3	±20%	Typ 19.7 Max 20.7	Typ 7.2	Typ 11

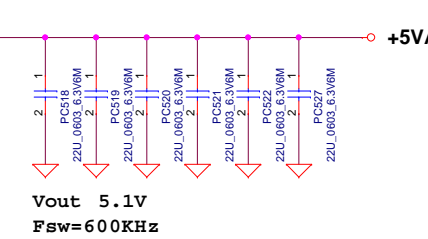


3VALWP
TDC 5.2A
Peak Current 7.5A
OCP Current 8.0A (fix)

Non AR
3VALWP
TDC 5.5A
Peak Current 7.5A
OCP Current 8.0A (fix)

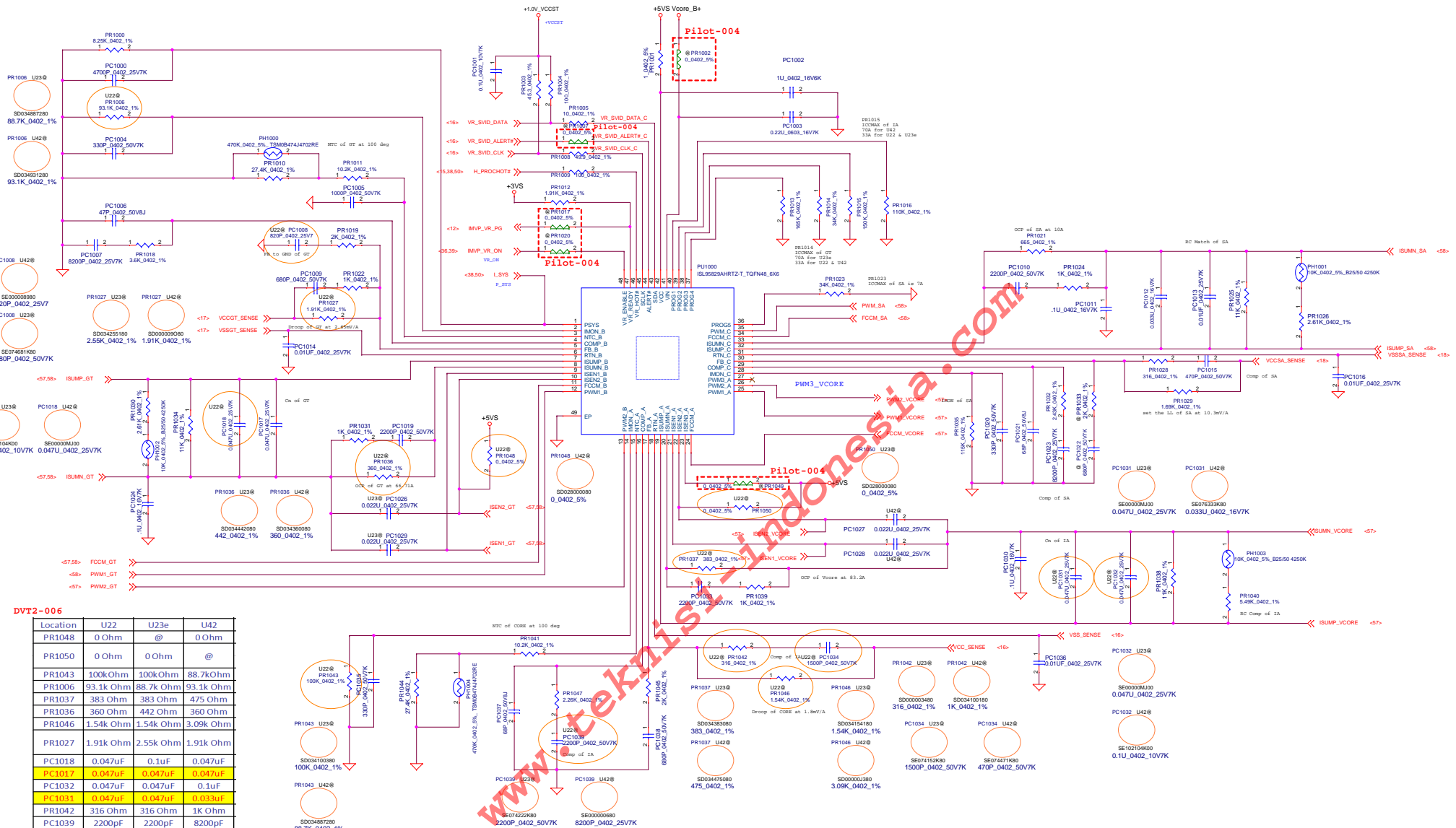


5VALWP
TDC 7.9A
Peak Current 11.0A
OCP Current 13.0A



3V/5V controller(35.1), Support component(35.2)

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Issued Date	2014/10/17	Deciphered Date	2014/12/05	Title
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				Document Number
				LA-E671P
				Rev
				0.4
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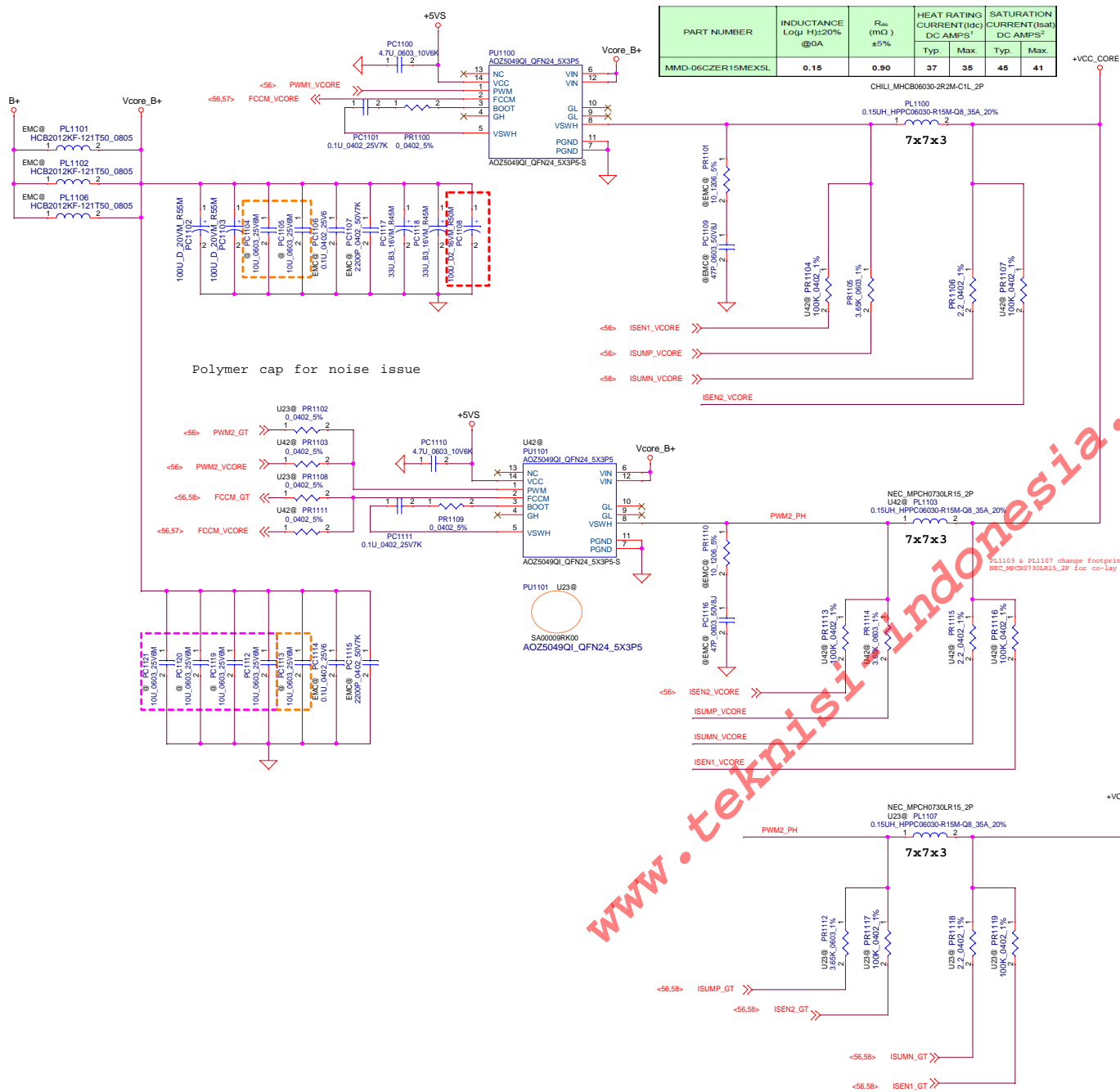


DVT2-006

Location	U22	U23e	U42
PR1048	0 Ohm	@	0 Ohm
PR1050	0 Ohm	0 Ohm	@
PR1043	100k Ohm	100k Ohm	88.7k Ohm
PR1006	93.1k Ohm	88.7k Ohm	93.1k Ohm
PR1037	383 Ohm	383 Ohm	475 Ohm
PR1036	360 Ohm	442 Ohm	360 Ohm
PR1046	1.54k Ohm	1.54k Ohm	3.09k Ohm
PR1027	1.91k Ohm	2.55k Ohm	1.91k Ohm
PC1018	0.047uF	0.1uF	0.047uF
PC1017	0.047uF	0.047uF	0.047uF
PC1032	0.047uF	0.047uF	0.1uF
PC1031	0.047uF	0.047uF	0.033uF
PR1042	316 Ohm	316 Ohm	1K Ohm
PC1039	2200pF	2200pF	8200pF
PR1040	5.49 KOhm	5.49 KOhm	5.49 KOhm
PC1034	1500pF	1500pF	470pF
PC1008	820pF	680pF	820pF

CPU Vcore controller(36.1), Drivers(36.2), Support component(36.3)
Acoustic Noise B+ Bulk CAR(37.2)

Security Classification	2014/10/17	Compal Secret Data	2014/12/05
Issued Date	Deciphered Date		
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Title		Compal Electronics, Inc.	
Size		Vcore IS195829	
Date		Tuesday, October 07, 2017	
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PART NUMBER	INDUCTANCE Loq (μH)±20% @0A	R _{dc} (mΩ) ±5%	HEAT RATING CURRENT (dc) DC AMPS ¹		SATURATION CURRENT (Isat) DC AMPS ²	
			Typ.	Max.	Typ.	Max.
MMD-06CZER15MEXSL	0.15	0.90	37	35	45	41

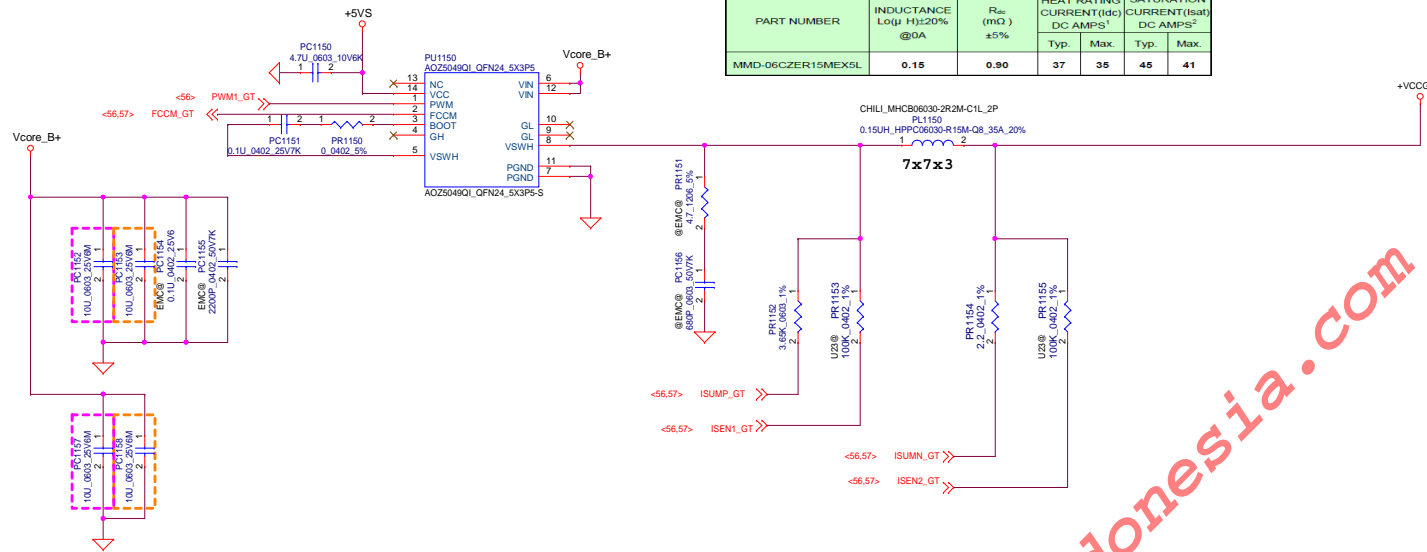
	KBL-RU42 rev.1.6 PAG	KBL-U22 (GT1/GT2) rev.1.5 EDS rev.1.6 PAG	KBL-U23e rev.1.5 EDS rev.1.6 PAG
IA+ring ICCM64	29/32	29	
IA+ring TDC	42	21	
IA+ring di[A]	55	25	
IA+ring DC/A2.4	2.4	2.4	
GT ICCMAX	28	31	64 for merged VR
GT TDC[A]	18	18	38 for merged VR
GT di[A]	20	28	46
GT DC/AC L	3.1	3.1	2
SA ICCMAX	5	4.5	5.1
SA DC/AC L	10.3	10.3	10.3
PL2 extreme	51	29/32	43
PL4 extreme	71	51	66

CPU_Vcore controller(36.1), Drivers(36.2), Support component(36.3)
CPU_Core output CAP(36.4), Acoustic Noise B+ B+ k CAP(37.2)

VCC_GT (U-line 22)
TDC 18A
Peak Current 31A
OCP current 37A

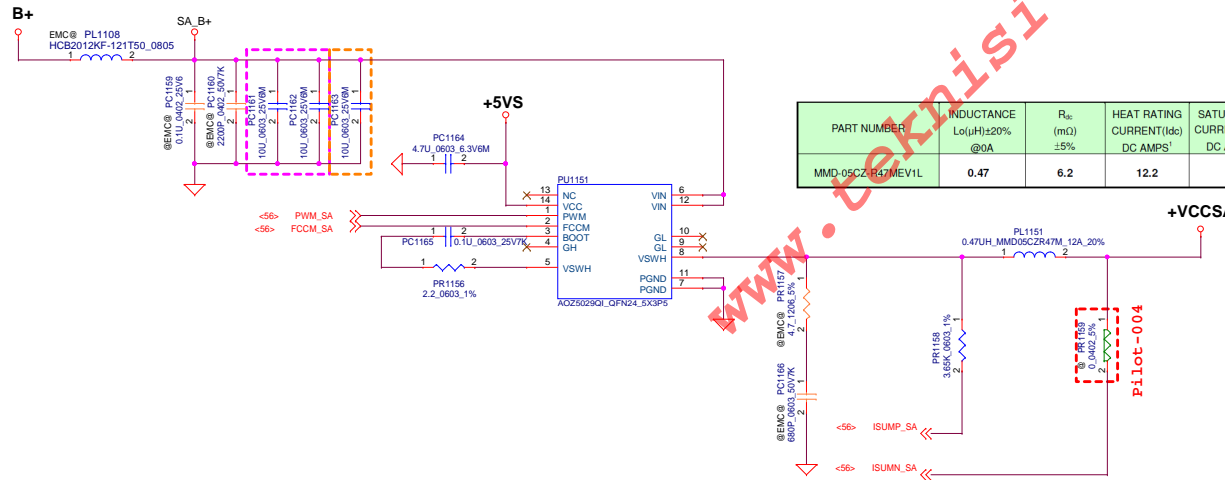
VCC_GT Merged(GT+GTx)(U-line 23e)
TDC 35A
Peak Current 64A
OCP current 74A

PART NUMBER	INDUCTANCE Lo(μ H) \pm 20% @0A	R _{dc} (m Ω) \pm 5%	HEAT RATING CURRENT(I _{dc}) DC AMPS ²	SATURATION CURRENT(I _{sat}) DC AMPS ²
MMD-06CZER15MEX5L	0.15	0.80	Typ. 37 Max. 35	Typ. 45 Max. 41



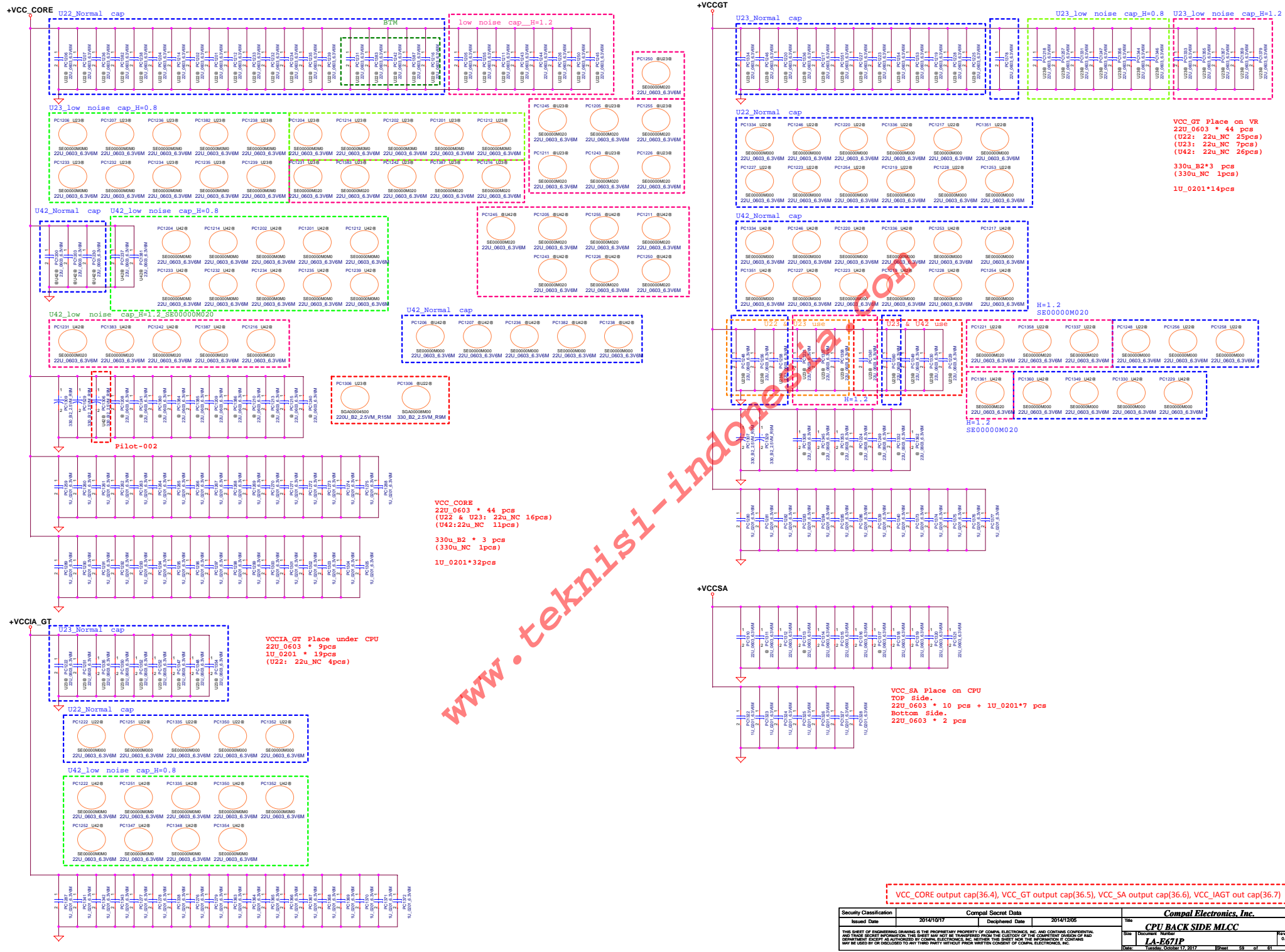
PART NUMBER	INDUCTANCE Lo(μ H) \pm 20% @0A	R _{dc} (m Ω) \pm 5%	HEAT RATING CURRENT(I _{dc}) DC AMPS ²	SATURATION CURRENT(I _{sat}) DC AMPS ²
MMD-05CZ-R47MEV1L	0.47	6.2	12.2	16

VCC_SA
TDC 5A
Peak Current 5.1A
OCP current 7A

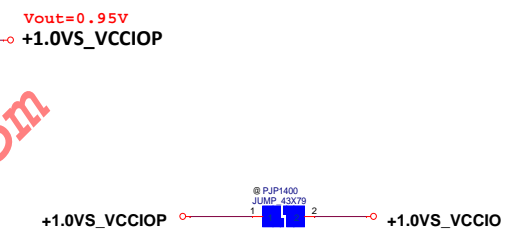
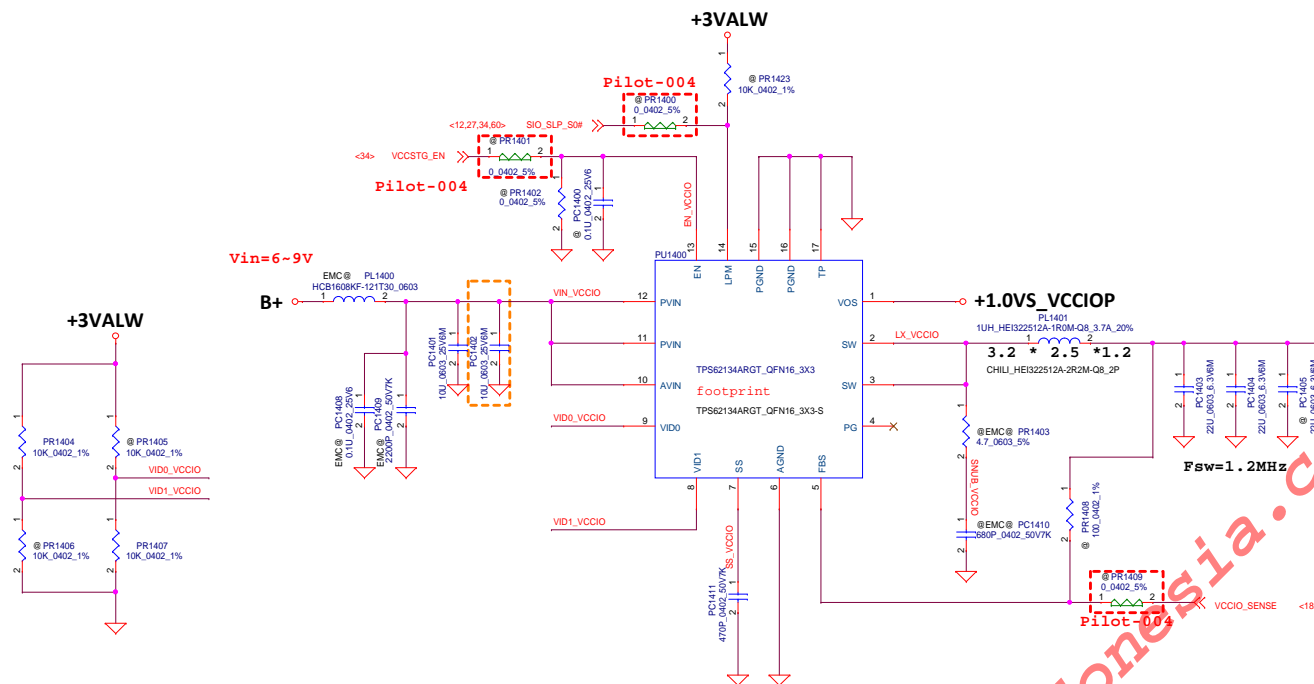


CPU_Vcore controller(36.1), Drivers(36.2), Support component(36.3),
GFX output CAP(36.5)

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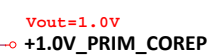
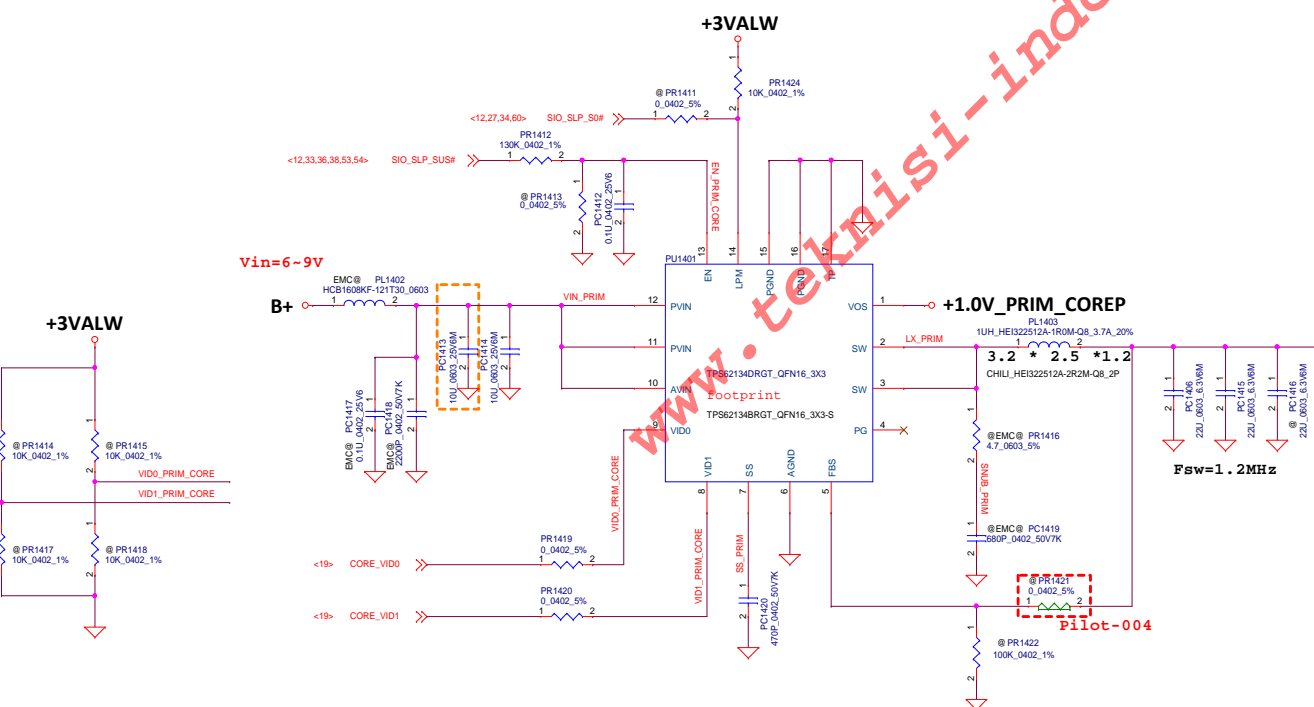
	LPM	VID1	VID0	Vout
TPS62134A VCCIO	0	X	X	0.000 (LPM)
	1	0	0	0.850
	1	0	1	0.8750
	1	1	0	0.950
	1	1	1	0.975



VCCIO
TDC 2.2A
Peak Current 3.1 A
OCP Current 4.2 A Fix by IC
MIN:3.6A
MAX:4.9A
Choke DCR 34.0mohm



PRIM_CORE
TDC 1.8A
Peak Current 2.6 A
OCP Current 4.2 A Fix by IC
MIN:3.6A
MAX:4.9A
Choke DCR 34.0mohm



	LPM	VID1	VID0	Vout
TPS62134D PRIM_CORE	0	X	X	0.700 (LPM)
	1	0	0	0.850
	1	0	1	0.900
	1	1	0	0.950
	1	1	1	1.000

+1.0VS_VCCIO controller(35.21), Support component(35.22)
+1.0V_PRIM_CORE controller(35.23), Support component(35.24)

LPM	VID1	VID0	Vout
0	X	X	0.000 (LPM)
1	0	0	0.800
1	0	1	0.950
1	1	0	1.000
1	1	1	1.050



+VCC_EDRAM_P

+VCC_EDRAM
TDC 1.75A
Peak Current 2.5 A
OCP Current 4.2 A Fix by IC
MIN:3.6A
MAX:4.9A
Choke DCR 34.0mohm

+VCC_EOPIO_P

+VCC_EOPIO
TDC 1.4A
Peak Current 2.0 A
OCP Current 4.2 A Fix by IC
MIN:3.6A
MAX:4.9A
Choke DCR 34.0mohm

LPM	VID1	VID0	Vout
0	X	X	0.000 (LPM)
1	0	0	0.800+0.05
1	0	1	0.950+0.05
1	1	0	1.000+0.05
1	1	1	1.050+0.05

2015/12/16 Add PR1530 PR1531 for Kabylake EOPIO support to 0.85V
2016/02/04 Change PR1531 from 6.2k to 5.1k to Set 0.85V and 1 V

+VCC_EDRAM controller(35.25), Support component(35.26)
+VCC_EOPIO controller(35.27), Support component(35.28)